Product Description

ATEK950P6 is a sub-octave switchable filter bank covering 485 – 8000 MHz frequency band. Filterbank consists of an SP8T switch followed by 7 fixed frequency band pass filters which are followed by another SP8T switch. 8th arms of each SP8T switch are used to send the input/output signals to 2 pins. This allows users to bypass the filterbank off-chip. Alternatively, additional off-chip filter or filterbanks can be implemented by using the bypass feature.

RF Input and Outputs are internally matched to 50 ohms for ease of use.

Filterbank provides 43 dBm IIP3 which allows users to realize high dynamic range wideband receiver frontends. Sub-octave filterbank architecture improves overall system IIP2.

Filterbank is housed in 6x6 mm low-cost surface mount package.

Evaluation Board, custom package and module options are available upon request.

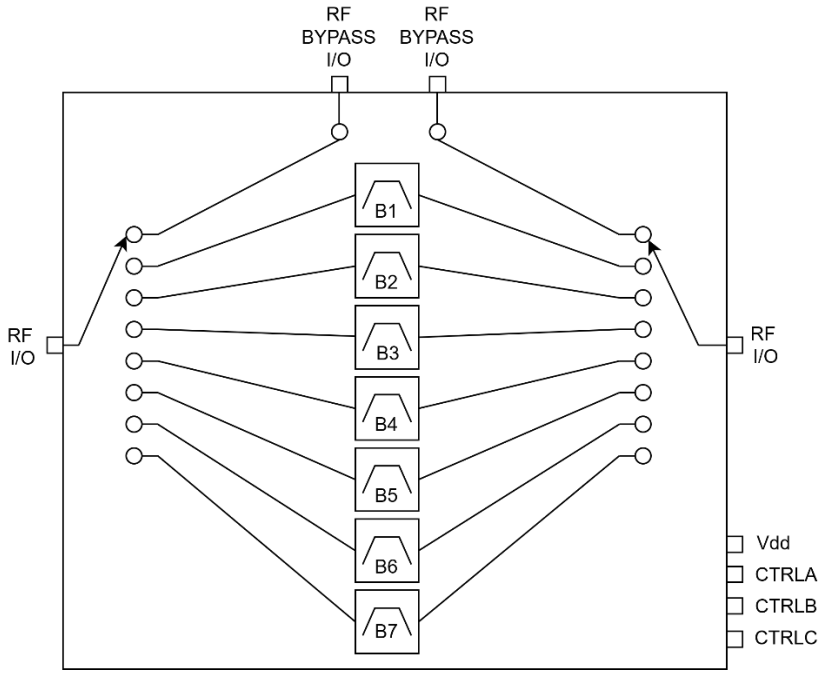
Product Features

- Frequency Range: 485 – 8000 MHz
- 7 Switchable Band Pass Filters
- IIP3: 43 dBm
- Single Supply: 3.3 V to 5 V

Applications

- Test Equipment
- Electronic Warfare
- Wideband Receivers
- Spectrum Analysis
- SDR

Functional Block Diagram



Electrical Specifications

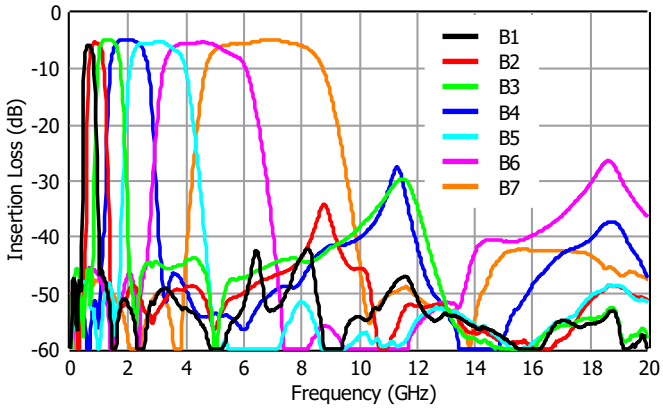
Test conditions unless otherwise noted: V_{dd} = +5 V, T = 25 C.

Parameter		Min	Typ	Max	Units
Frequency Range		2		8000	MHz
3dB Bandwidth (High Pass 3dB cutoff – Low Pass 3dB cutoff)	Band 1		485 - 810		MHz
	Band 2		670 – 1125		
	Band 3		960 – 1670		
	Band 4		1440 - 2560		
	Band 5		2140 - 3850		
	Band 6		3300 - 5880		
	Band 7		4820 - 8500		
	External Bypass		2-9000		
Insertion Loss	Filter Paths		6		dB
	External Bypass Path		3		
Input IP3			43		dBm
Input P1dB			27.5		dBm
Switching Speed			150		nS
Logic Level	Low	0		0.5	V
	High	2		5	
DC Supply Voltage (V_{DD})		3.2	5	5.5	V
DC Supply Current (I_{DD})			11.5		mA
Control Supply Current (I_{CTRLA} + I_{CTRLB} + I_{CTRLC})			2		mA
Operating Temperature		-55		105	°C

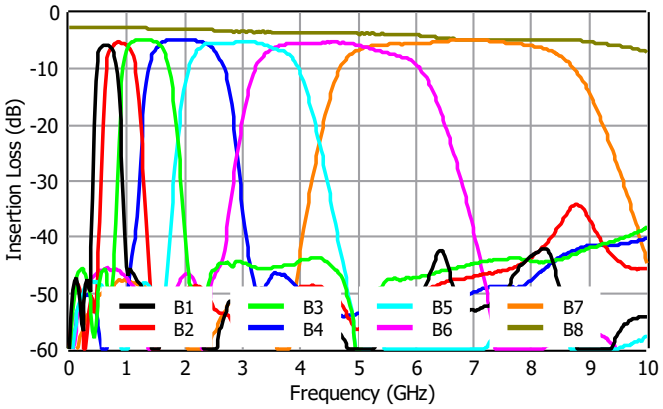
Typical Performance Plots

Conditions unless otherwise specified: V_{dd} = +5 V, T = 25 C.

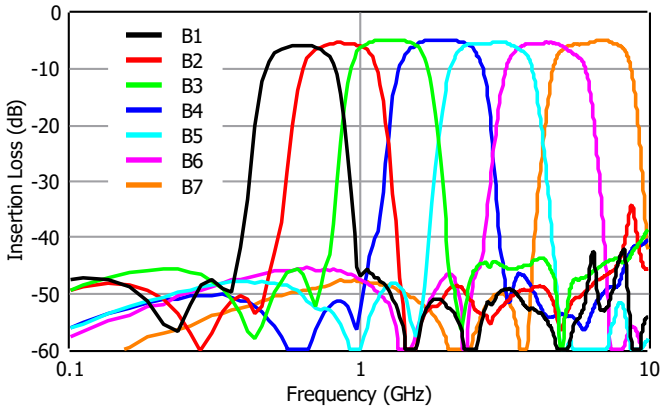
S21, Vdd=5 V



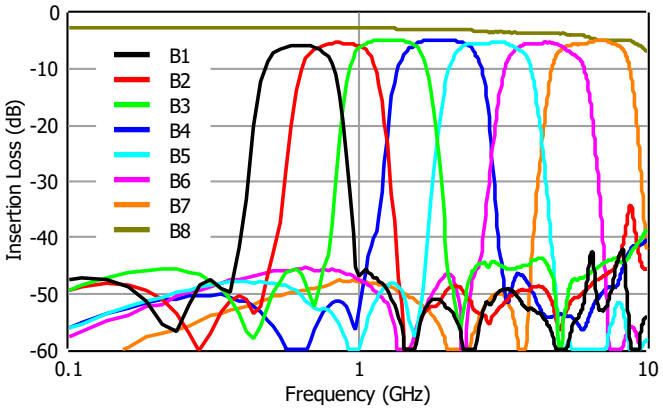
S21, Vdd=5 V



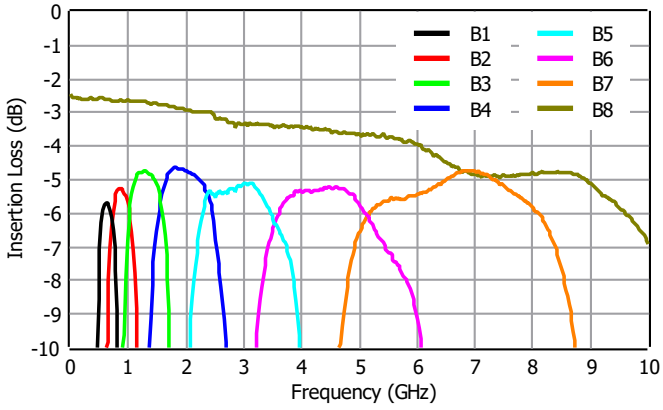
S21, Vdd=5 V, Log Scale



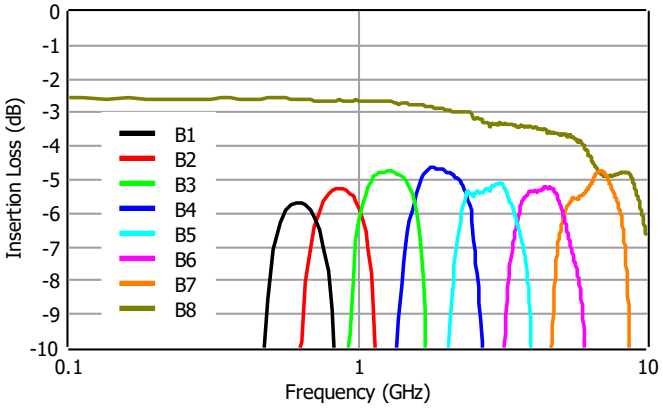
S21, Vdd=5 V, Log Scale



S21, Vdd=5 V



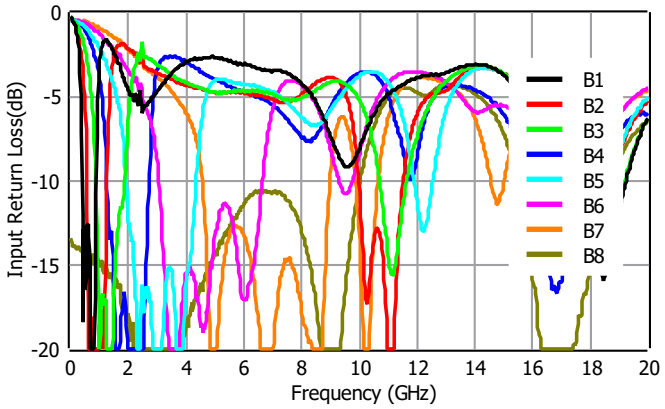
S21, Vdd=5 V, Log Scale



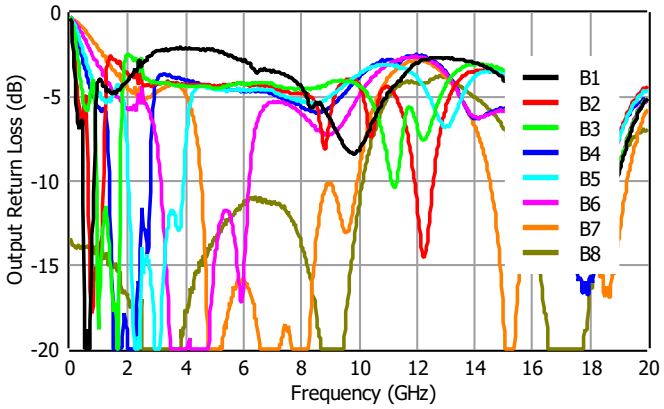
Typical Performance Plots

Conditions unless otherwise specified: V_{dd} = +5 V, T = 25 C.

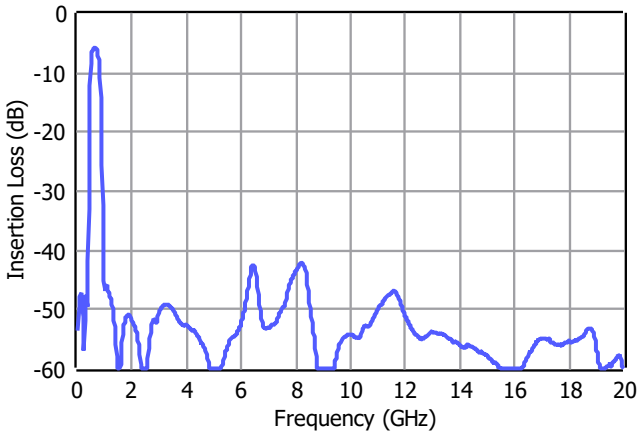
S11, Vdd=5 V



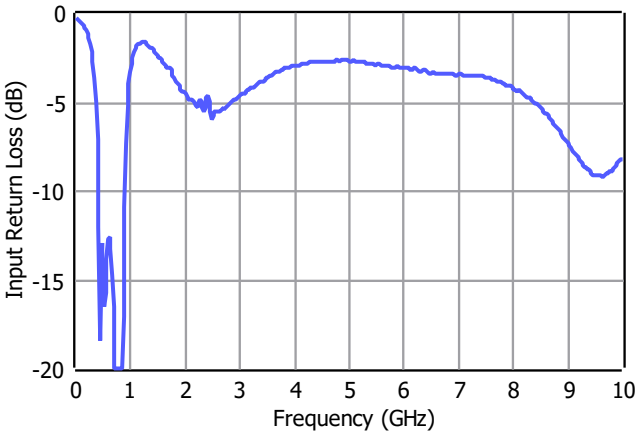
S22, Vdd=5 V



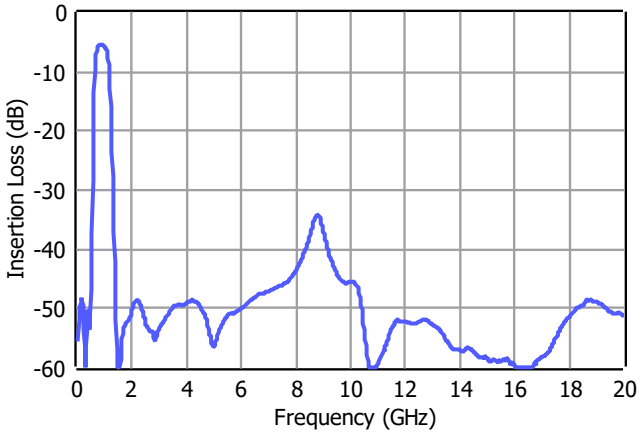
Band1 S21



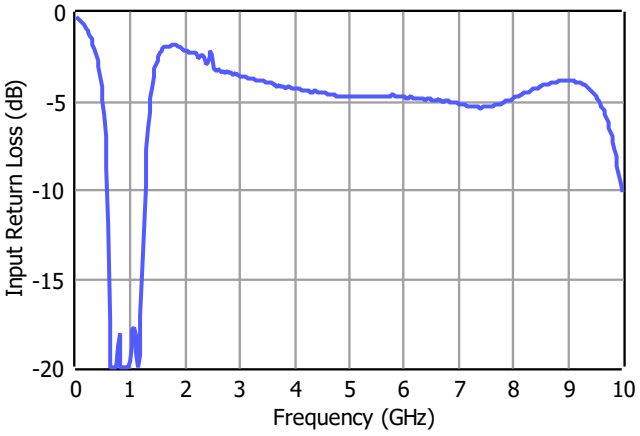
Band1 S11



Band2 S21



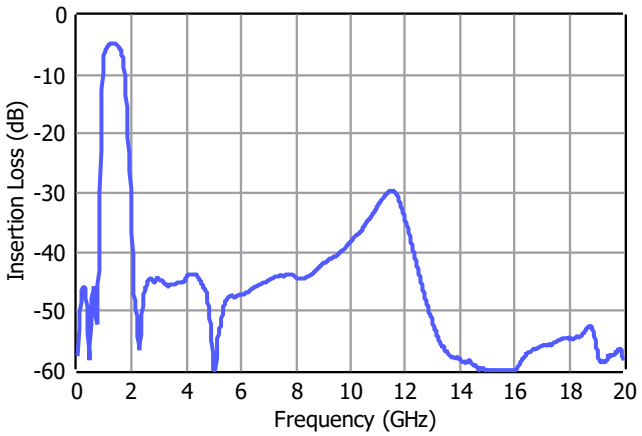
Band2 S11



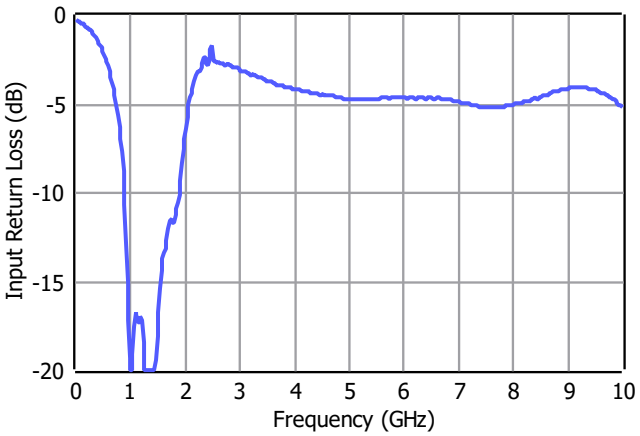
Typical Performance Plots

Conditions unless otherwise specified: V_{dd} = +5 V, T = 25 C.

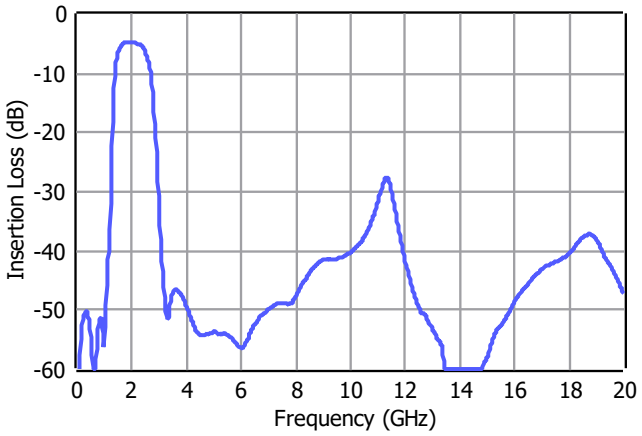
Band3 S21



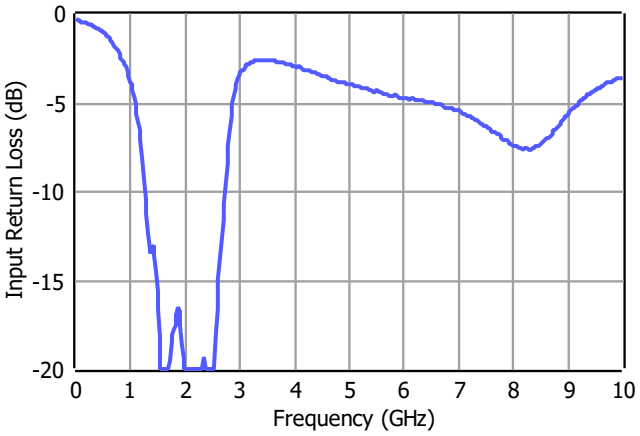
Band3 S11



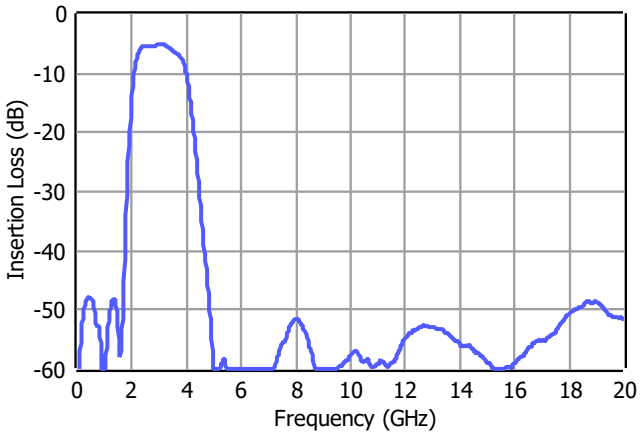
Band4 S21



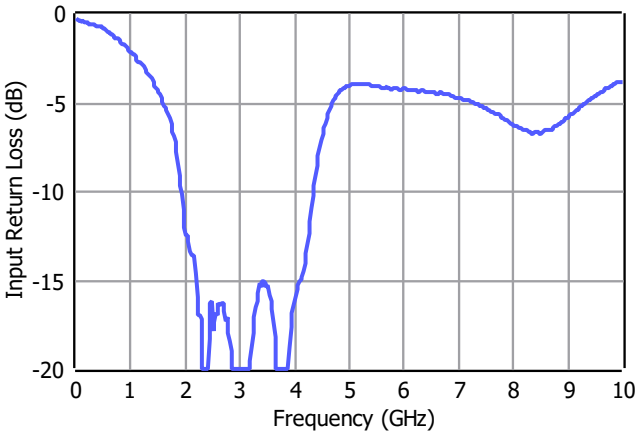
Band4 S11



Band5 S21



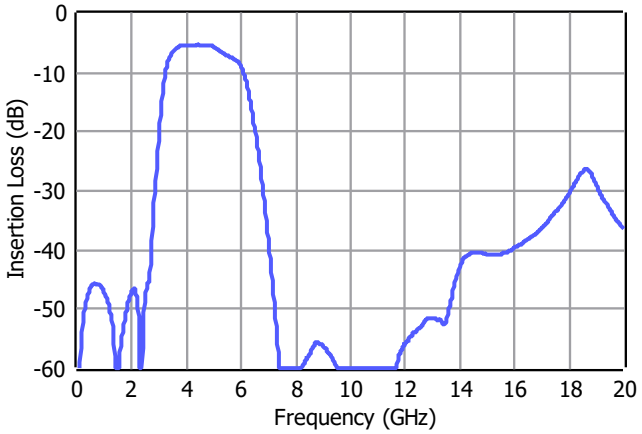
Band5 S11



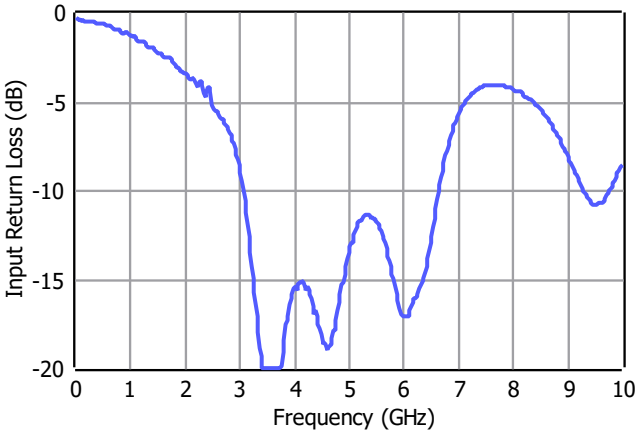
Typical Performance Plots

Conditions unless otherwise specified: V_{dd} = +5 V, T = 25 C.

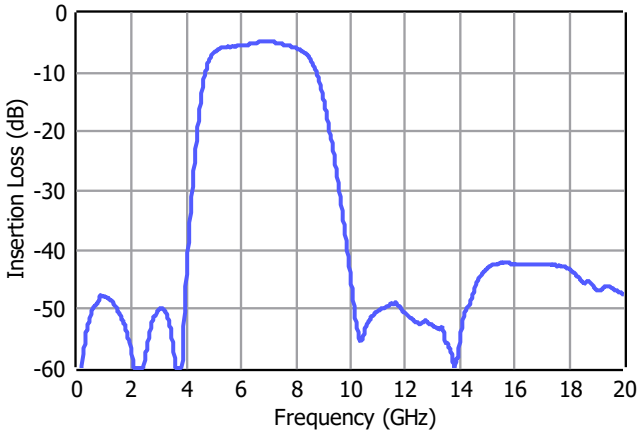
Band6 S21



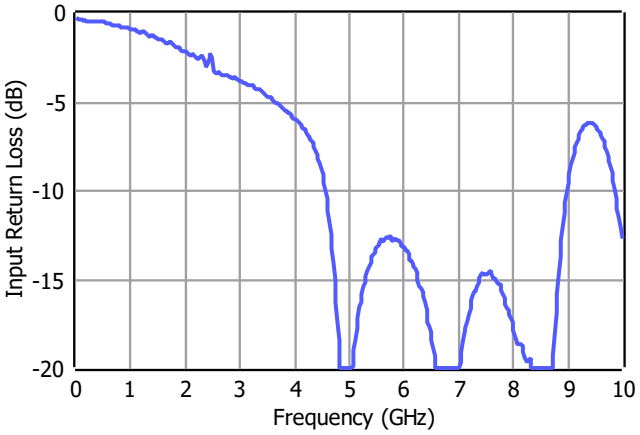
Band6 S11



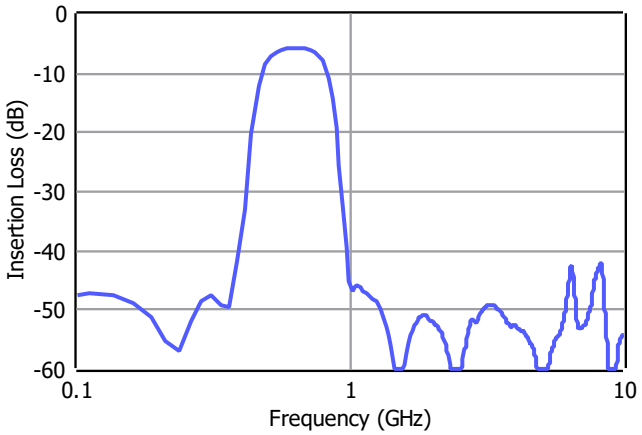
Band7 S21



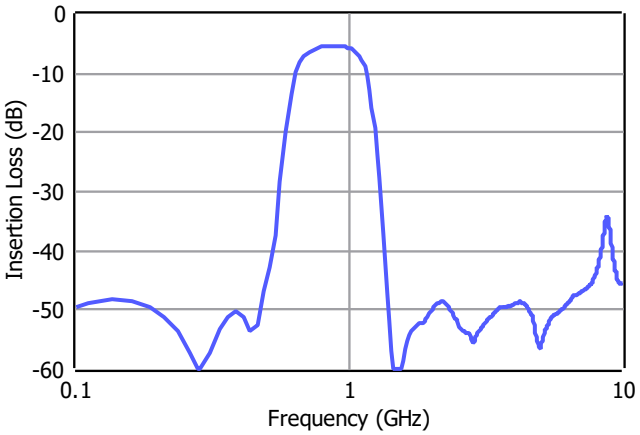
Band7 S11



Band1 S21, Log Scale



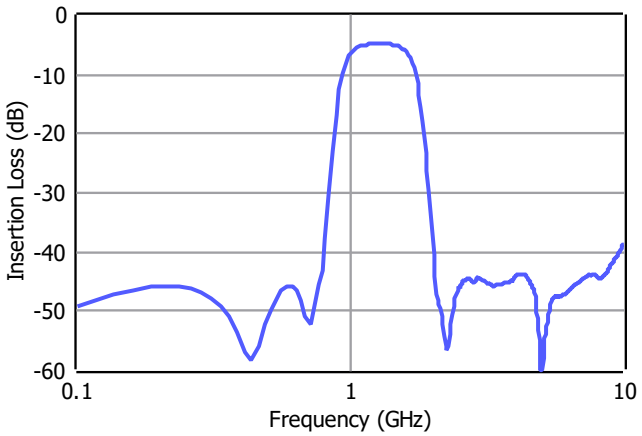
Band2 S21, Log Scale



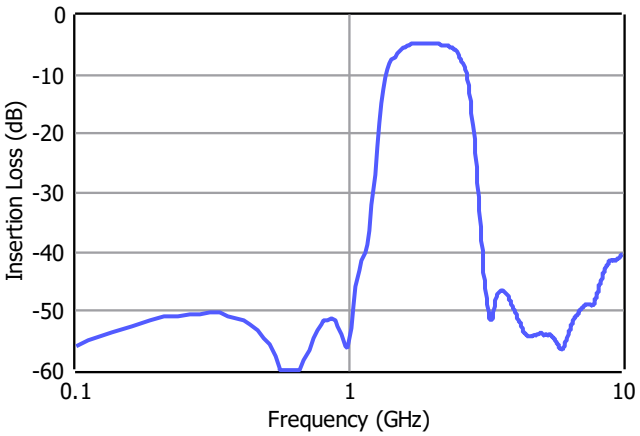
Typical Performance Plots

Conditions unless otherwise specified: V_{dd} = +5 V, T = 25 C.

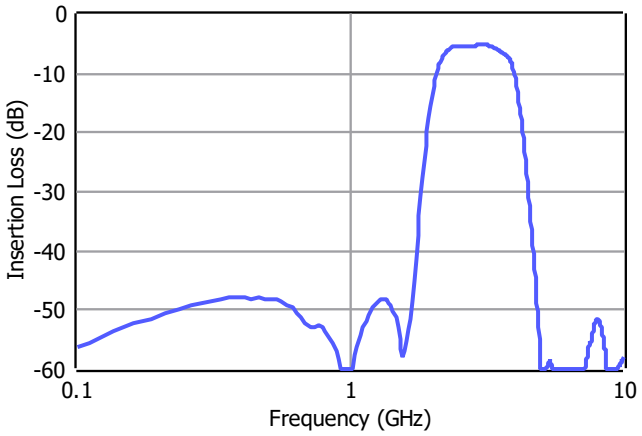
Band3 S21, Log Scale



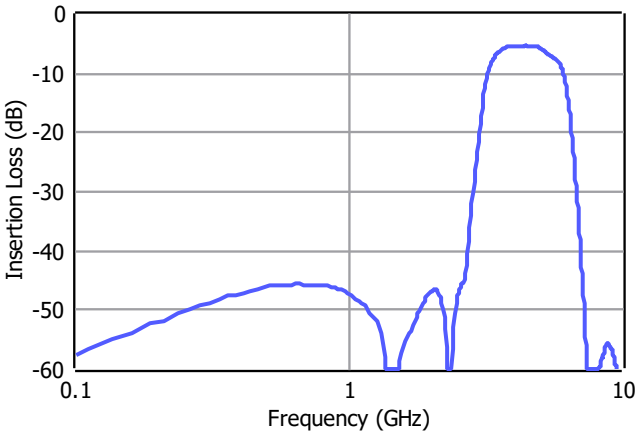
Band4 S21, Log Scale



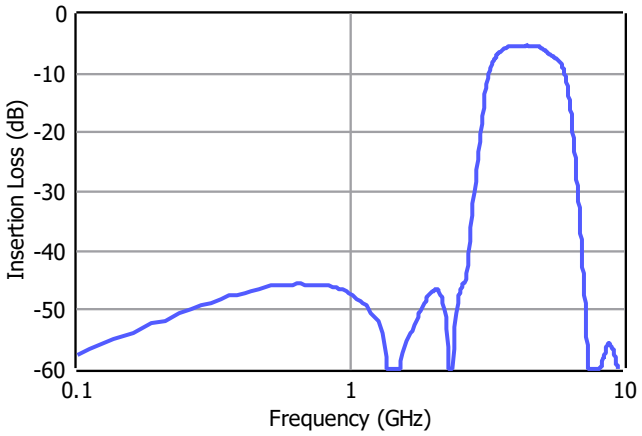
Band5 S21, Log Scale



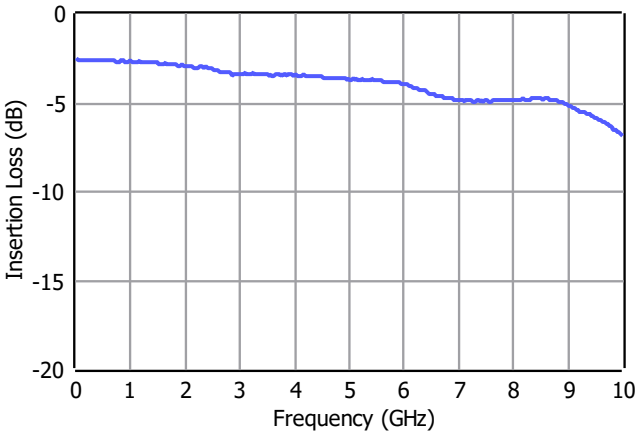
Band6 S21, Log Scale



Band7 S21, Log Scale



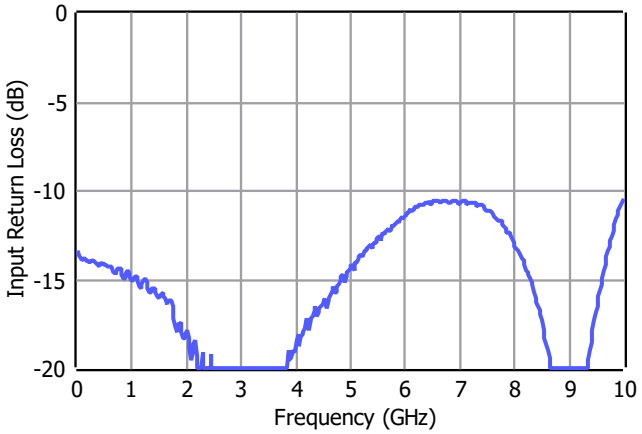
Thru Path S21



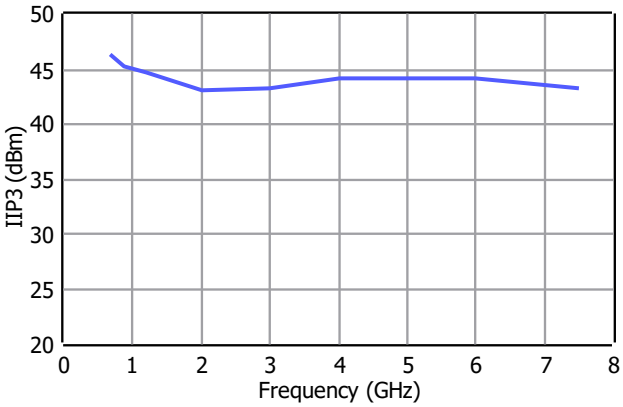
Typical Performance Plots

Test conditions unless otherwise specified: V_{dd} = +5 V, T = 25 C.

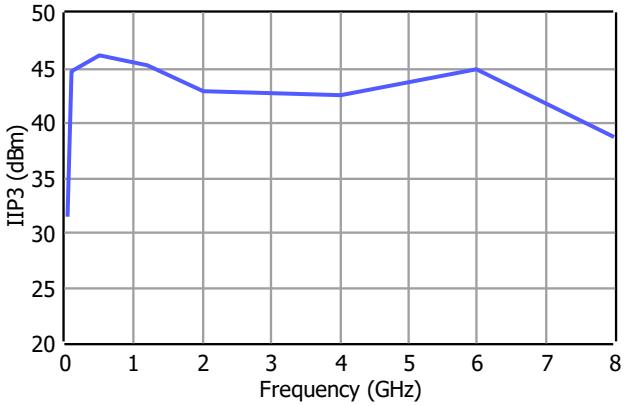
Thru Path S11



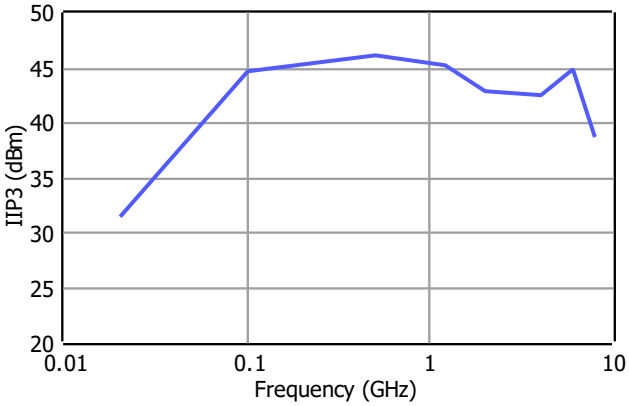
Input IP3, Filter Path



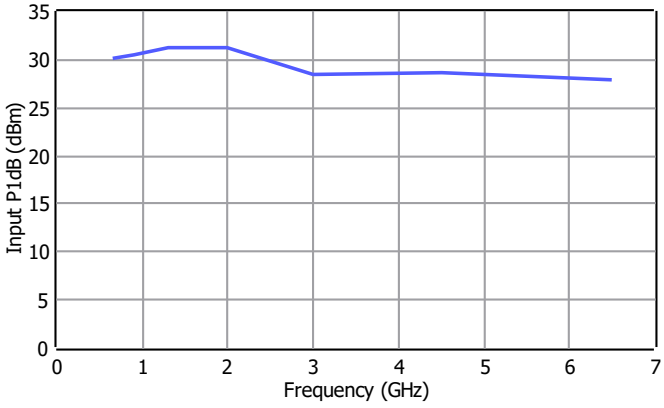
Input IP3 Thru Path



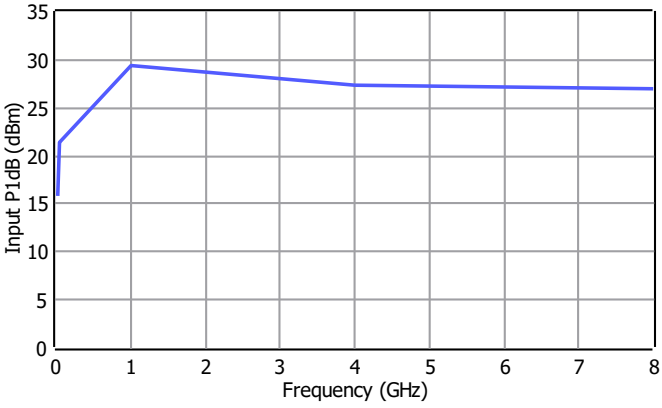
Input IP3 Thru Path, Log Scale



Input P1dB, Filter Path



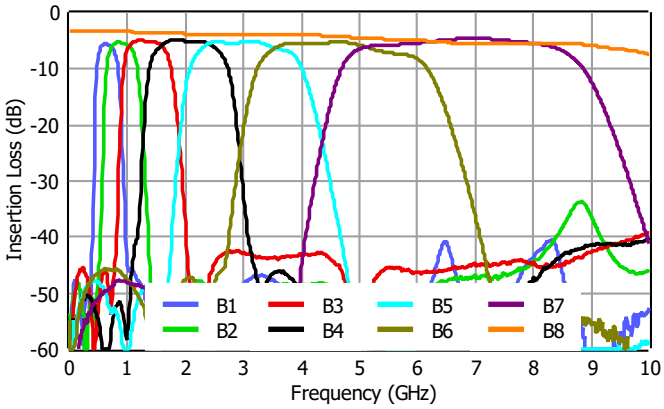
Input P1dB Bypass Path



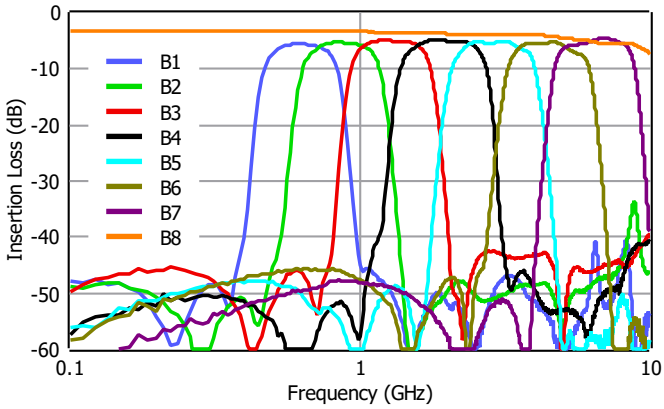
Typical Performance Plots

Test conditions unless otherwise specified: V_{dd} = +5 V, T = -55 C, -40 C, 25 C, 85 C, 105 C.

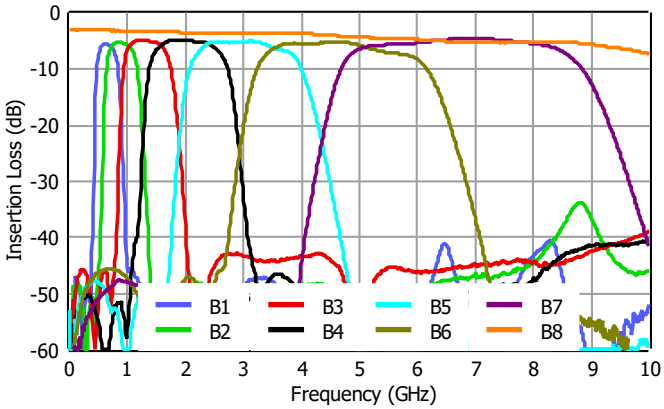
S21, Vdd=5 V, -55 C Temperature



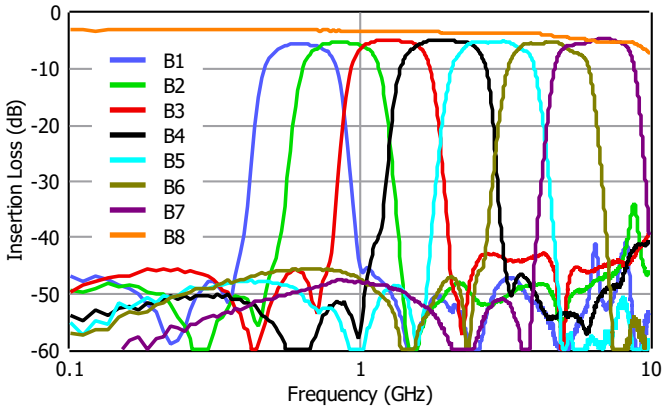
S21, Vdd=5 V, -55 C Temperature, Log Scale



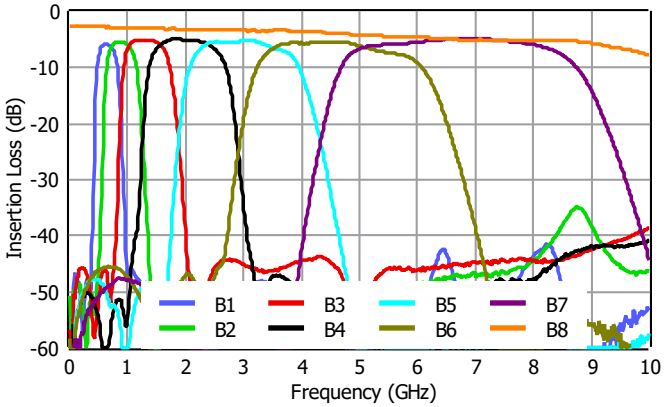
S21, Vdd=5 V, -40 C Temperature



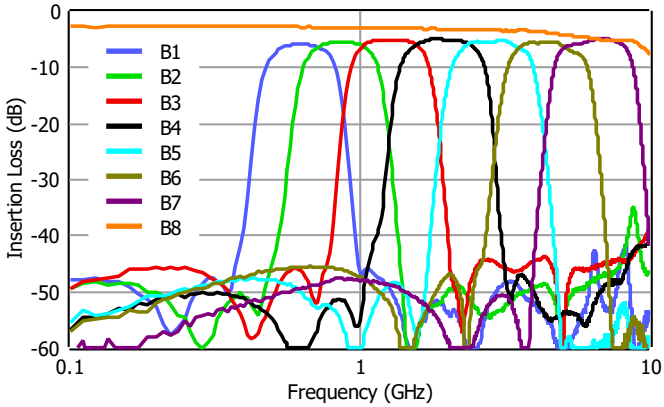
S21, Vdd=5 V, -40 C Temperature, Log Scale



S21, Vdd=5 V, 25 C Temperature



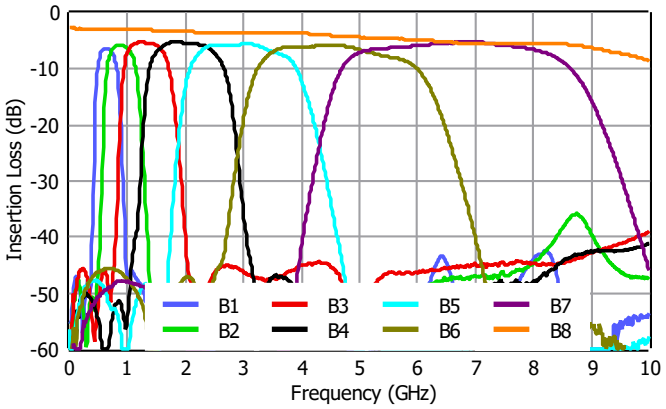
S21, Vdd=5 V, 25 C Temperature, Log Scale



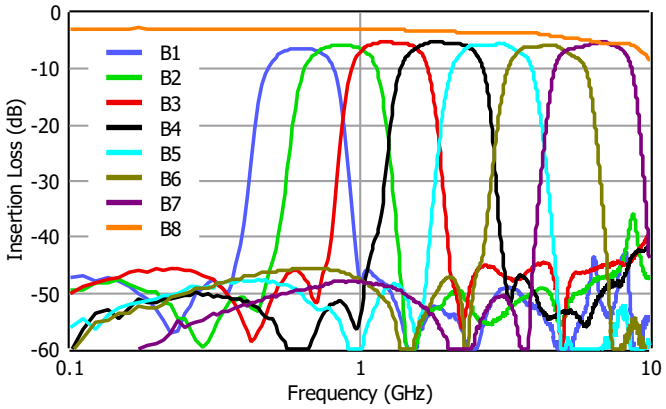
Typical Performance Plots

Test conditions unless otherwise specified: V_{dd} = +5 V, T = -55 C, -40 C, 25 C, 85 C, 105 C.

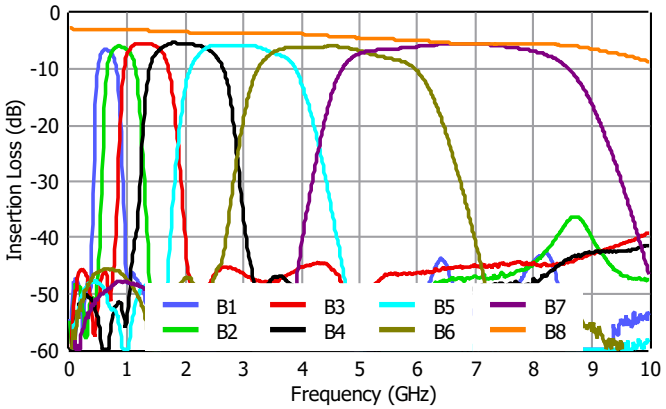
S21, Vdd=5 V, 85 C Temperature



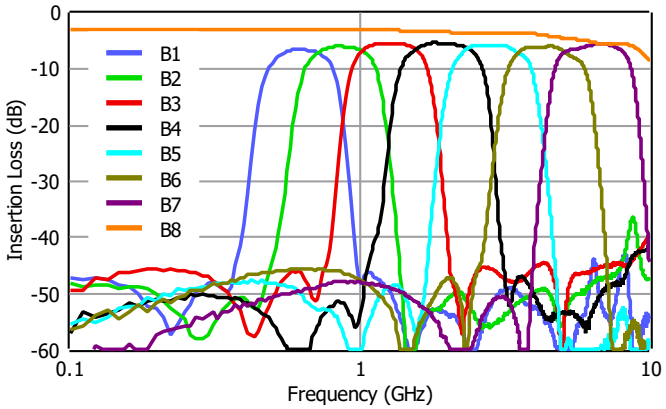
S21, Vdd=5 V, 85 C Temperature, Log Scale



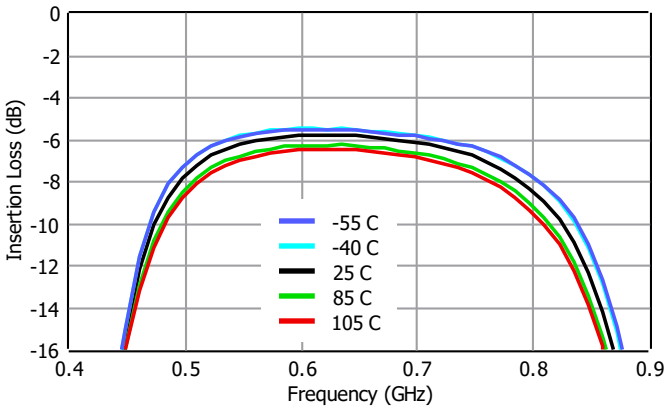
S21, Vdd=5 V, 105 C Temperature



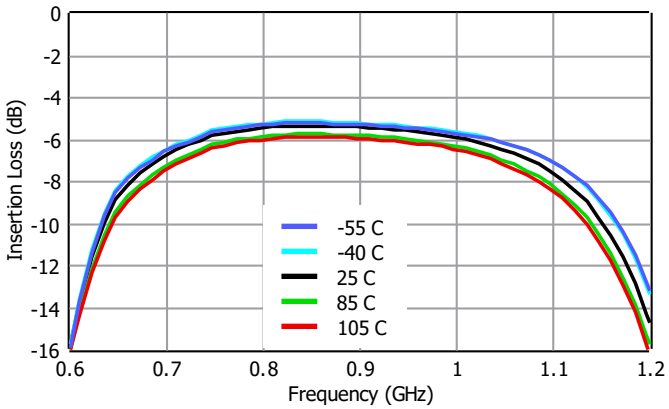
S21, Vdd=5 V, 105 C Temperature, Log Scale



Band1 S21 vs Temperature



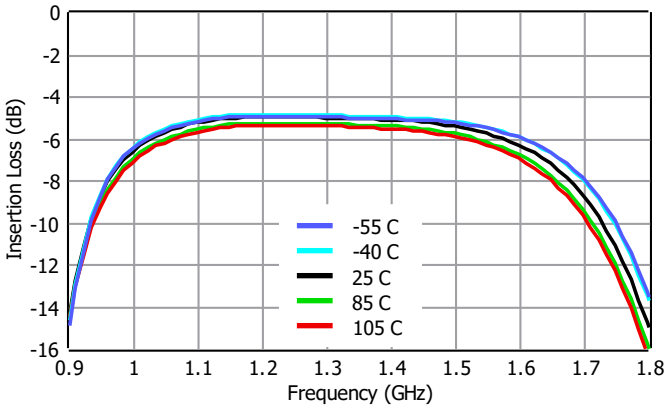
Band2 S21 vs Temperature



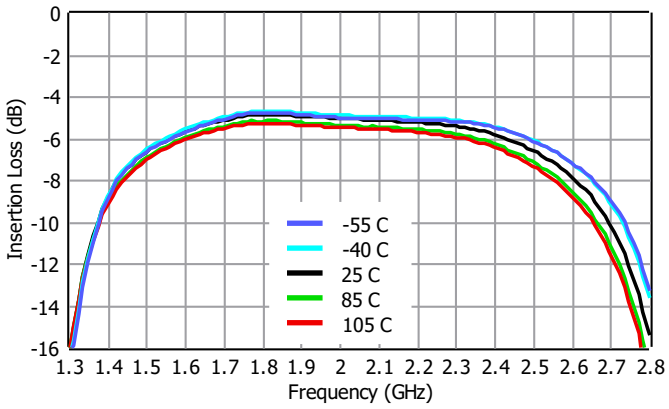
Typical Performance Plots

Test conditions unless otherwise specified: V_{dd} = +5 V, T = -55 C, -40 C, 25 C, 85 C, 105 C.

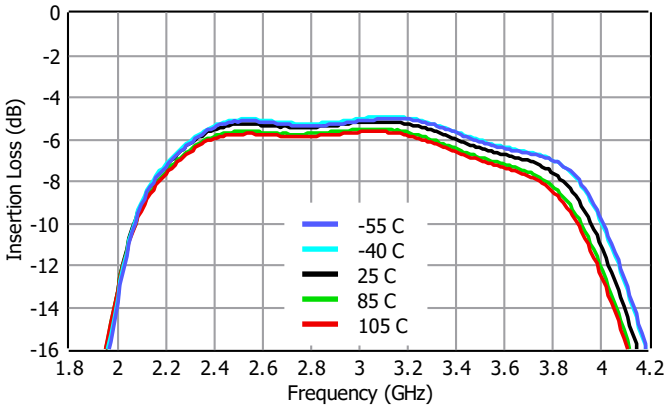
Band3 S21 vs Temperature



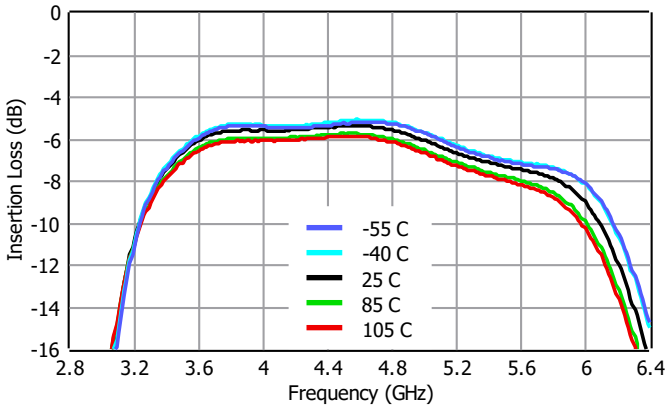
Band4 S21 vs Temperature



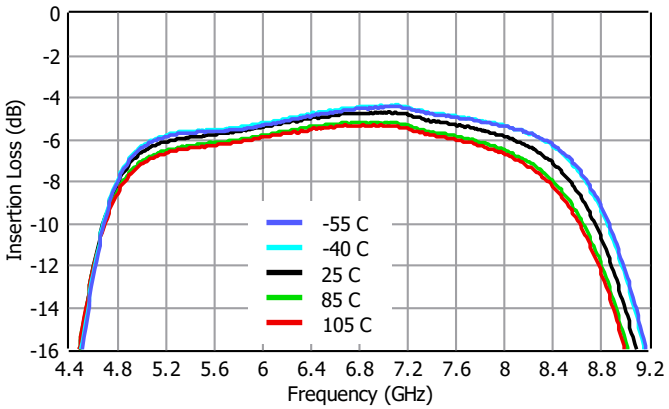
Band5 S21 vs Temperature



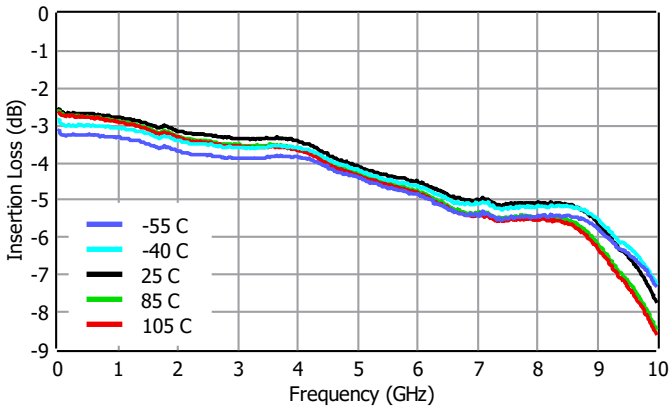
Band6 S21 vs Temperature



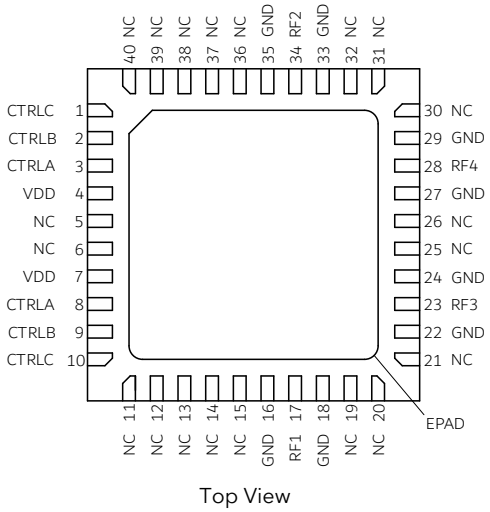
Band7 S21 vs Temperature



Band8 S21 vs Temperature



Pin Description



Top View

Pin Number	Pin Name	Description
17	RF1	RF pin. Can be used as input or output. DC coupled; external DC block capacitors are required.
34	RF2	RF pin. Can be used as input or output. DC coupled; external DC block capacitors are required.
23	RF3	RF pin. Can be used as input or output. DC coupled; external DC block capacitors are required. If unused should be left open
28	RF4	RF pin. Can be used as input or output. DC coupled; external DC block capacitors are required.
1, 10	CTRLC	Control C input. Two CTRLC pins are shorted internally. Using one of them is sufficient for controlling filter state.
2, 9	CTRLB	Control B input. Two CTRLB pins are shorted internally. Using one of them is sufficient for controlling filter state.
3, 8	CTRLA	Control A input. Two CTRLA pins are shorted internally. Using one of them is sufficient for controlling filter state.
4, 7	VDD	Supply input.
5, 6, 11-15, 19-21, 25, 26, 30-32, 36-40	NC	These pins are not internally connected. Can be grounded on the PCB.
16, 18, 22, 24, 27, 29, 33, 35	GND	Ground.
41	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

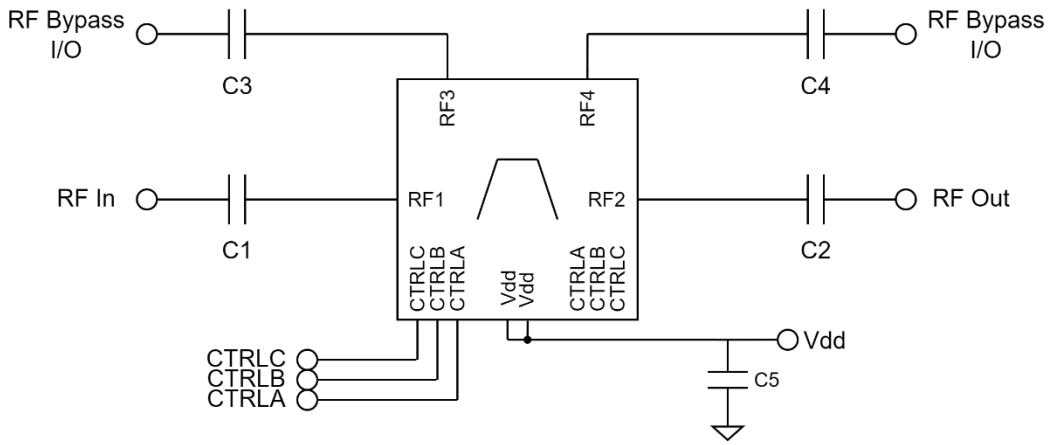
Control Interface

CTRLA	CTRLB	CTRLC	Filter Bank State
LOW	LOW	LOW	Band1
LOW	HIGH	HIGH	Band2
LOW	LOW	HIGH	Band3
HIGH	LOW	HIGH	Band4
LOW	HIGH	LOW	Band5
HIGH	LOW	LOW	Band6
HIGH	HIGH	LOW	Band7
HIGH	HIGH	HIGH	External Bypass State

Applications Information

Signal entering from RF1 pins goes into 8 selectable paths. 7 of these paths are fixed frequency band pass filters and the 8th path is routed to RF3 pin. Symmetrical architecture lies in between RF2 and RF4 pins. Thus, RF3 and RF4 pins can be used to add an off chip thru path on the PCB. This will allow user to add bypass feature to the filterbank. Alternatively, an 8th filter can be connected in between RF3 and RF4 pins. Similarly, RF3 and RF4 pins can be used to connect an alternative filterbank. This allows user to create filterbank configurations with higher filter count in a modular architecture.

Typical application schematic to operate the filterbank is given below.



C1, C2, C3 and C4 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss. If RF3 and RF4 pins are not used, then using C3 and C4 is not required.

C5 is used to filter out the ripples and unwanted signal coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If these topics are of no concern, then filterbank can be operated without C5.

Filterbank can be supplied in alternative packages and custom housing.

All measurement results presented on this document are gathered with connectorized EVB, where RF1 is input and RF2 is output.

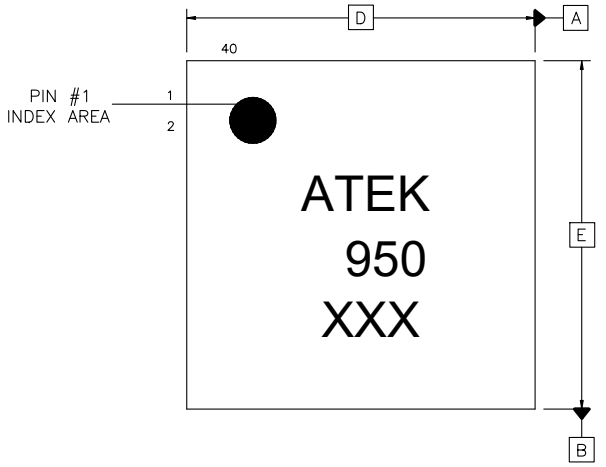
S21 data is de-embedded to eliminate the PCB trace loss and coaxial connector transition effects.

Absolute Maximum Ratings

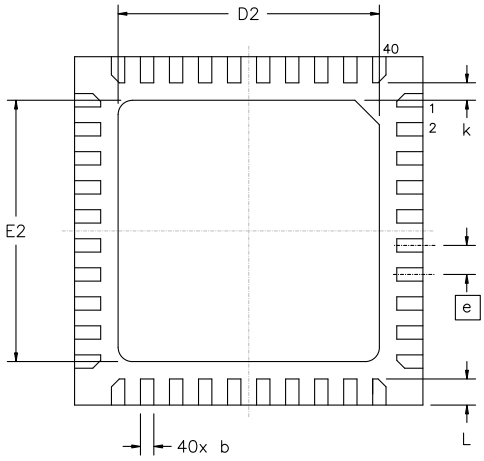
Parameter	Value/Range
Supply Voltage (V_{DD})	6 V
V_{CTRL} (V_{CTRLA}, V_{CTRLB}, V_{CTRLC}) If V_{CTRL}> V_{DD}, then V_{CTRL} – V_{DD} must be lower than 2V.	6 V
Supply Current I_{DD}	18 mA
Control Current (I_{CTRLA} + I_{CTRLB} + I_{CTRLC})	3 mA
Channel Temperature	150 °C
Thermal Resistance	90 °C/W
RF Input Power	+30 dBm
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

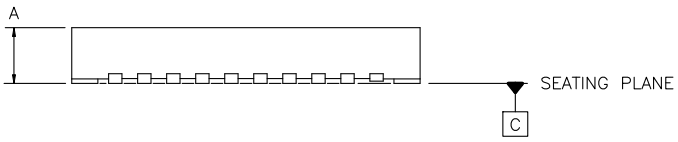
Mechanical and Marking Information



Top View



Bottom View



Side View

NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	4.40	4.60
b	0.18	0.30	e	0.50 BSC	
D	6.00 BSC		k	0.20	–
D2	4.40	4.60	L	0.40	0.50
E	6.00 BSC				

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	07.12.2021	Initial Release	
1.1	25.01.2022	Drawing and Plots Revised	3/7, 4/7, 5/7, 6/7
2.0	14.10.2022	Temperature Measurement Added	
2.1	01.11.2023	Format and Content Fixed	
2.2	11.11.2023	Format and Content Fixed	
2.3	14.08.2024	Large Signal Data Added and Application Section Revised	
2.4	08.02.2025	Current Added to Electrical Specifications Table	
2.5	24.02.2025	Current Added to Electrical Specifications Table	
2.6	05.03.2025	AMR Table Updated, Application Section Revised	
2.7	27.09.2025	Mechanical and Marking Information Updated	
2.8	03.10.2025	AMR Table Updated	