Product Description

ATEK900N3 is a wideband 2-bit Gain Equalizer with Switchable Gain Slope. Frequency of operation goes down to Low Frequency close to DC and goes up to 18 GHz.

ATEK900N3 operates with positive supply voltage and states are set by positive voltage control interface. Eliminating the need for external negative bias circuitry.

RF Input and output are matched to 50 ohms internally. This allows users to easily integrate the equalizer to wideband circuits.

Equalizer is housed in compact 3x3 mm low cost SMD package.

Evaluation Board, bare die, custom package, and module options are available upon request.

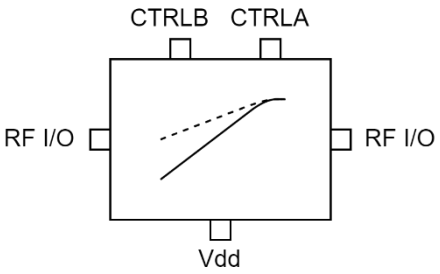
Product Features

- Frequency Range: LF - 18 GHz
- Switchable Slope
- Low Loss: 1 dB
- Single Supply
- 3x3 mm compact size

Applications

- Wideband Receivers
- SDR
- Test Equipment
- Telecommunications

Functional Block Diagram



Electrical Specifications

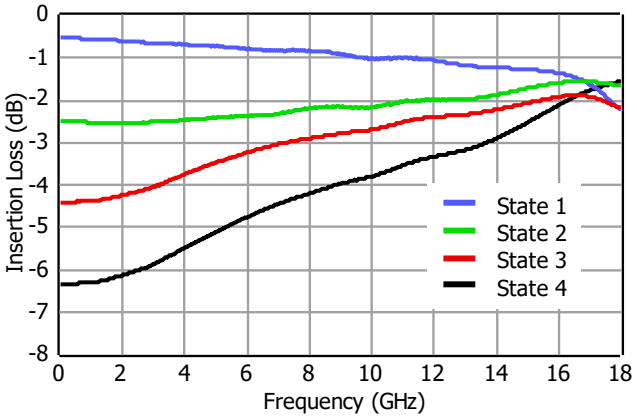
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		18	GHz
Insertion Loss (Thru State)	0.01 GHz		0.45		dB
	2 GHz		0.6		
	6 GHz		0.6		
	12 GHz		0.8		
	18 GHz		2.1		
Input Return Loss			18		dB
Output Return Loss			17		dB
Input P1dB			TBD		dBm
Input IP3		34	40		dBm
Switching Time	On		TBD	250	ns
	Off			250	
DC Supply Voltage (Vdd)			5		V
Current consumption (Vdd+CTRL)			2.5		mA
Control Voltage (CTRL)	Low		0		V
	High		5		
Operating Temperature		-40		85	°C

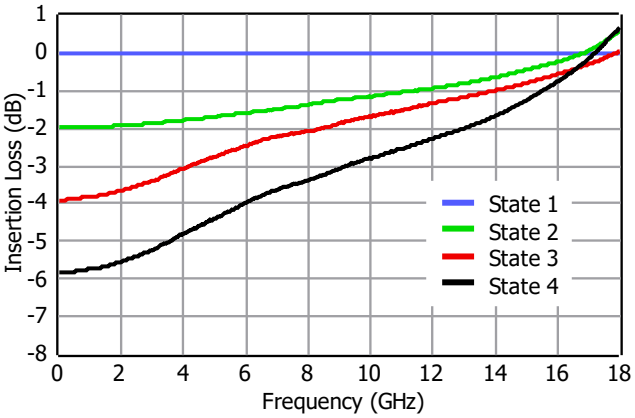
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

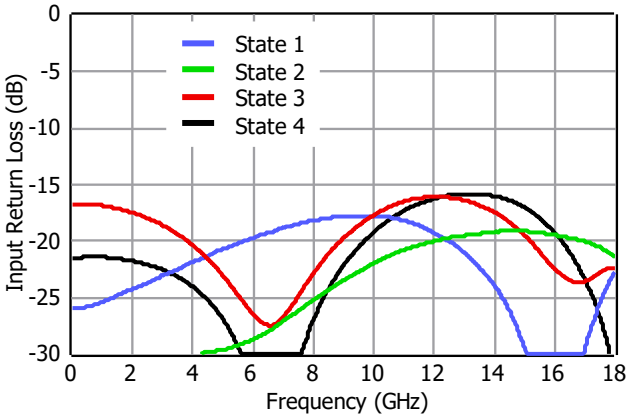
Insertion Loss



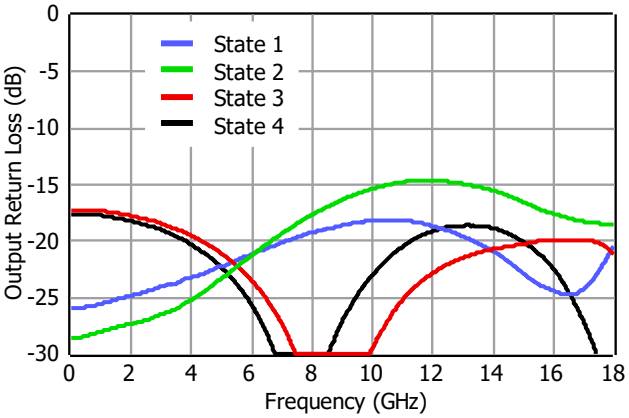
Normalized Equalization



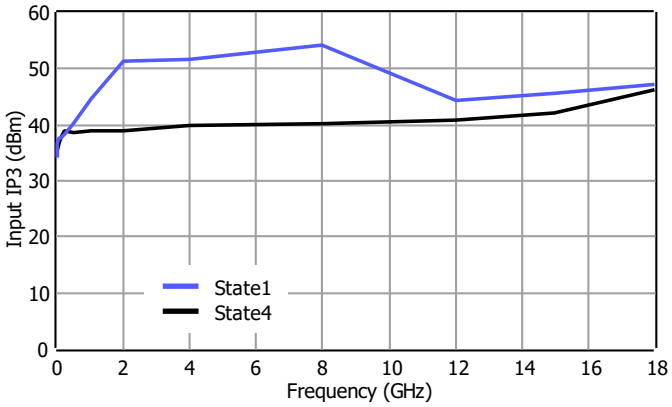
Input Return Loss



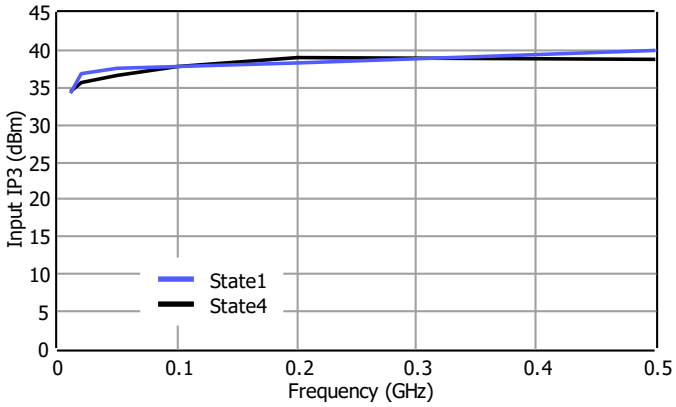
Output Return Loss



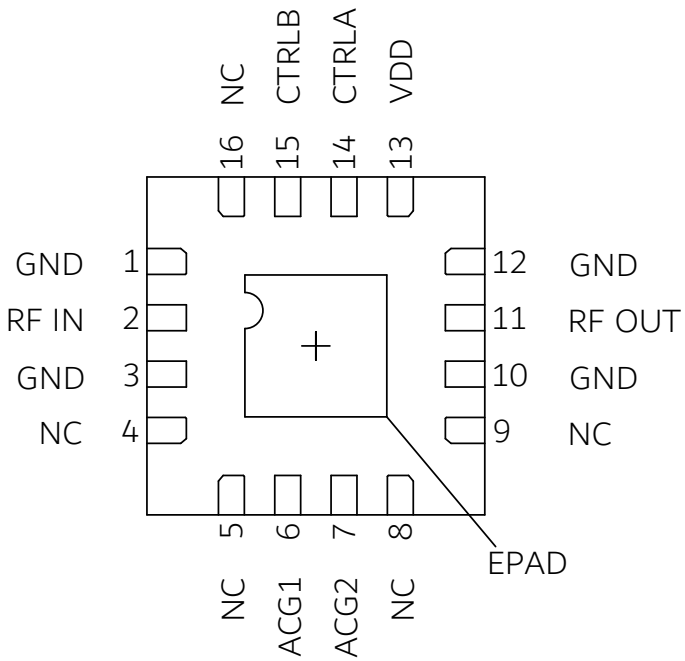
Input IP3



Input IP3 at Low Frequency



Pin Description



Top view

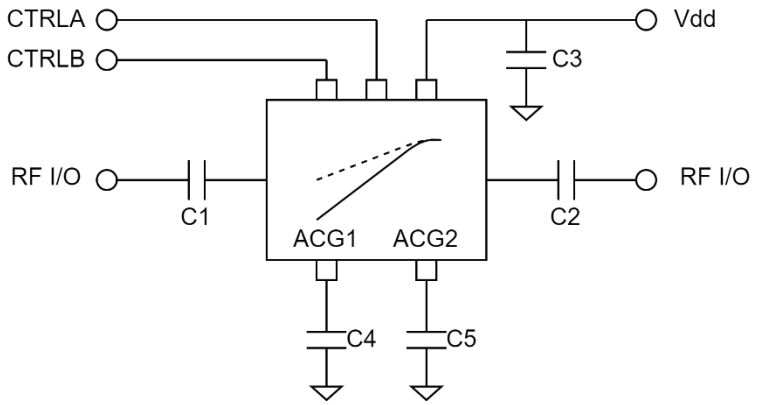
Pin Number	Pin Name	Description
2	RF IN	RF input/output pin. Wideband DC block capacitor is required.
11	RF OUT	RF input/output pin. Wideband DC block capacitor is required.
13	VDD	Vdd bias pin.
14	CTRLA	Control pin.
15	CTRLB	Control pin.
6	ACG1	AC ground pin. External shunt capacitor is required.
7	ACG2	AC ground pin. External shunt capacitor is required.
4, 5, 8, 9, 16	NC	These pins are not internally connected. Can be grounded on the PCB.
1, 3, 10, 12	GND	Ground.
17	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

State	CTRLA	CTRLB	Equalizer Slope
State 1	LOW	LOW	Thru
State 2	LOW	HIGH	2 dB
State 3	HIGH	LOW	4 dB
State 4	HIGH	HIGH	6 dB

Applications Information

Signal entering from RF IN goes to RF OUT with gain equalization. The slope of the gain equalization can be selected by using 2 control voltages.
Typical application schematic to operate the equalizer is given below.



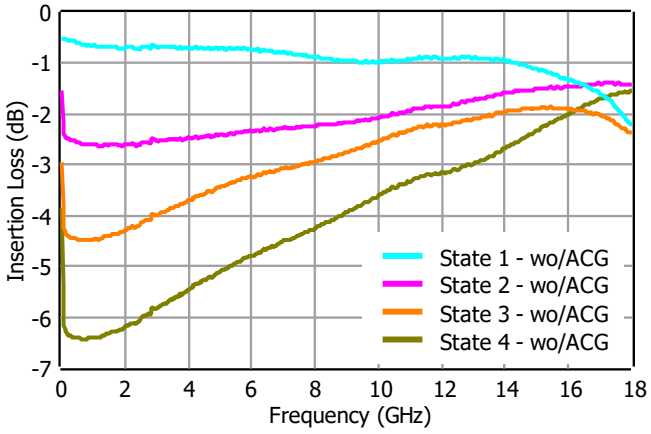
C1 and C2 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss.

C3 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C3 will improve this filtering. If this filtering is of no concern, then device can be operated without C3.

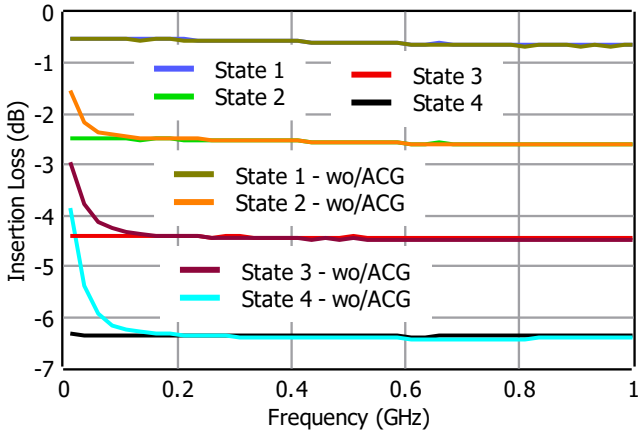
C4, and C5 are AC ground capacitors. Values of these capacitors should be chosen considering the lowest operation frequency of the application. 100 nF is used for ACG capacitors to generate the measurement results in this document.

If low frequency operation is not needed, then ACG capacitors can be removed. The S21 and S11 performance without the DC block capacitors are given below. These measurement are taken with the evaluation PCB.

Insertion Loss



Insertion Loss Low Frequency Region



Small signal plots in this document is generated with Probe PCB measurements with connectorized DC Block capacitors. ATEK900N3 is probed on the PCB to gather the data, to generate the s-parameter plots given in this document.

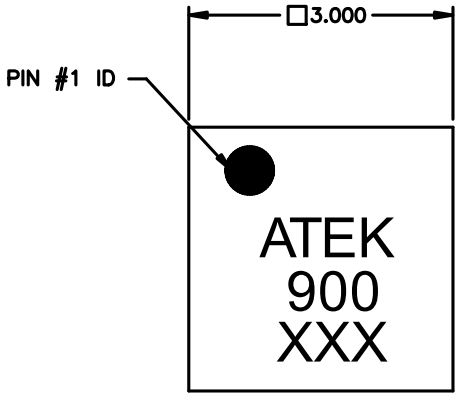
The NC pins of the equalizer are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

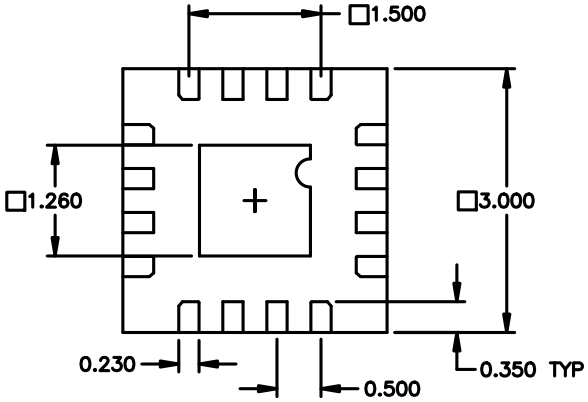
Parameter	Value/Range
Supply Voltage (Vdd)	TBD
Control Voltage (CTRLA, CTRLB)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

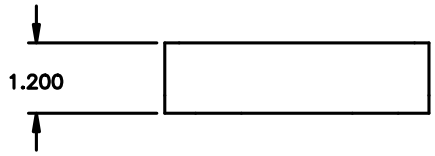
Mechanical and Marking Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES

1. ALL DIMENSIONS IN MM

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	25.10.2021	Initial Release	
1.1	21.03.2022	Plots Updated	
1.2	28.03.2023	Pin Description and Mechanical Drawing Updated	
1.3	31.08.2023	Plots Added	