

Product Description

ATEK569P5 is a wideband driver amplifier covering 0.2 to 24 GHz frequency range.

ATEK569P5 provides flat gain with single supply voltage. This allows users to easily realize wideband receiver frontends.

Amplifier housed in compact 5x5 mm low cost SMD package, input and output matched to 50 ohms internally. Evaluation Board, bare die, custom package, and module options are available upon request.

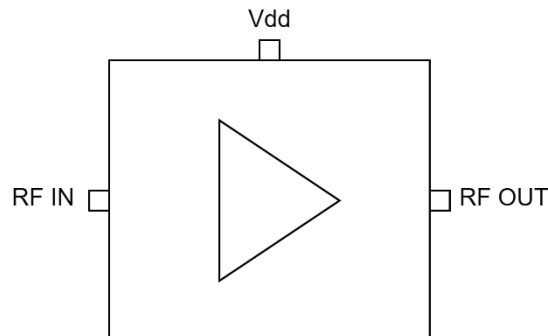
Product Features

- Frequency Range: 0.2 - 24 GHz
- Gain: 14 dB
- P1dB: 22.5 dBm
- IP3: 36 dBm
- Single Supply
- On-chip DC Block Capacitors
- 5x5 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test and Measurement
- SATCOM
- SDR

Functional Block Diagram



Electrical Specifications

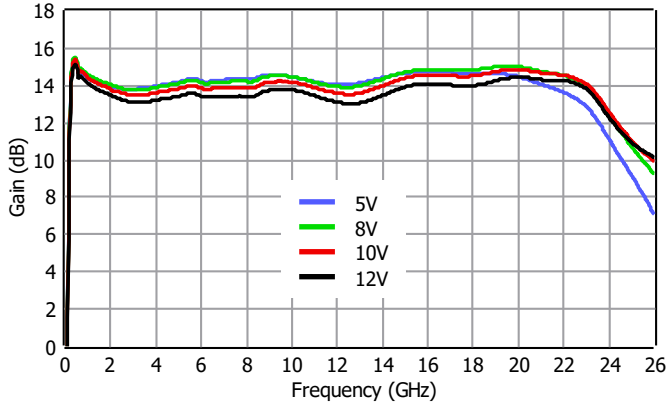
Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.2		24	GHz
Gain	0.25 GHz		13.8		dB
	2 GHz		13.4		
	8 GHz		13.4		
	12 GHz		13.1		
	18 GHz		13.9		
	24 GHz		12.2		
Isolation	0.25 GHz		60		dB
	2 GHz		52		
	8 GHz		38		
	12 GHz		34		
	18 GHz		27		
	24 GHz		25		
Input Return Loss			-20		dB
Output Return Loss			-15		dB
Noise Figure at 5V			3		dB
Output IP3			36		dBm
Output P1dB			22.5		dBm
Psat			25		dBm
DC Supply Voltage (Vdd)			10 12		V
DC Supply Current			150 160		mA
Operating Temperature		-40		85	°C

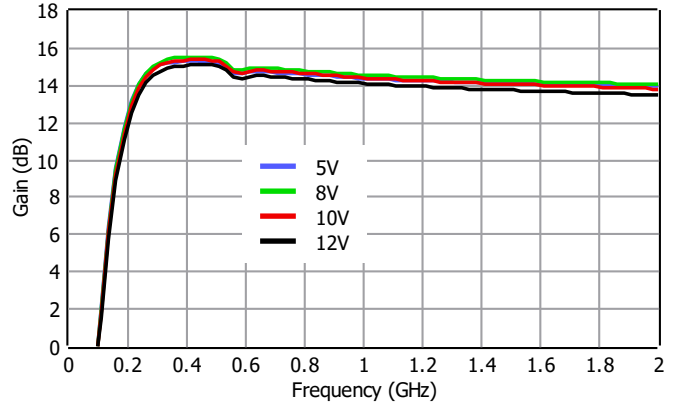
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

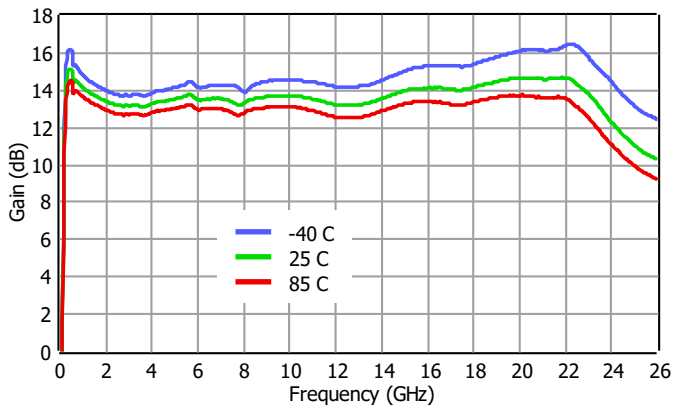
Gain



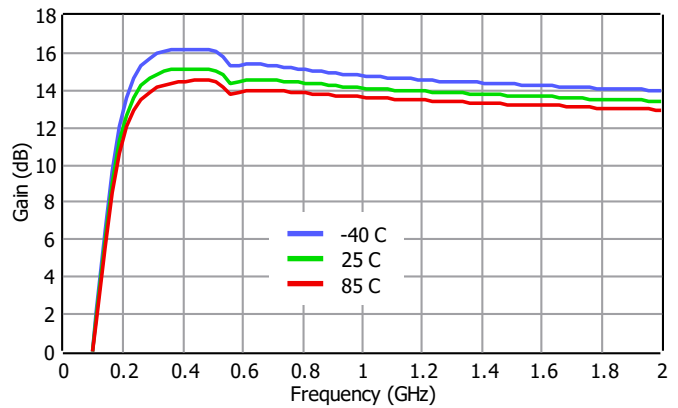
Gain at Low Frequency



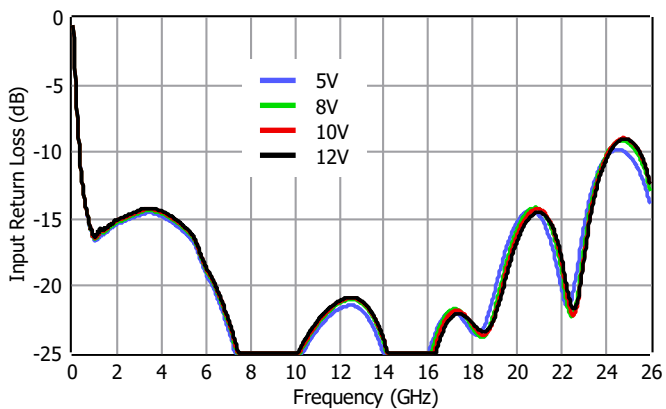
Gain vs Temperature



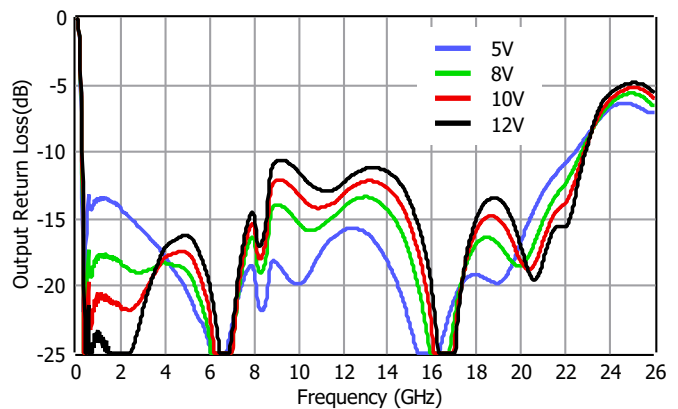
Gain vs Temperature at Low Frequency



Input Return Loss



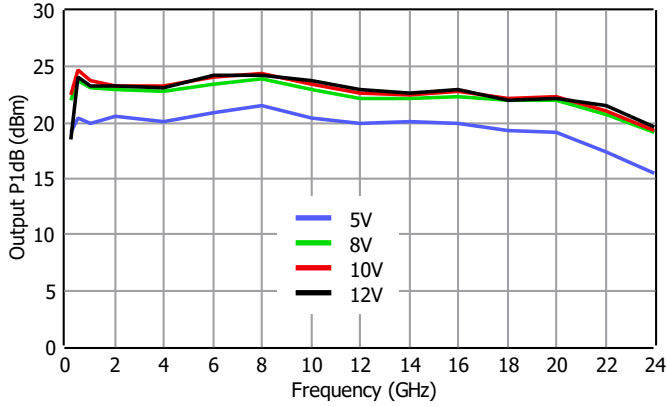
Output Return Loss



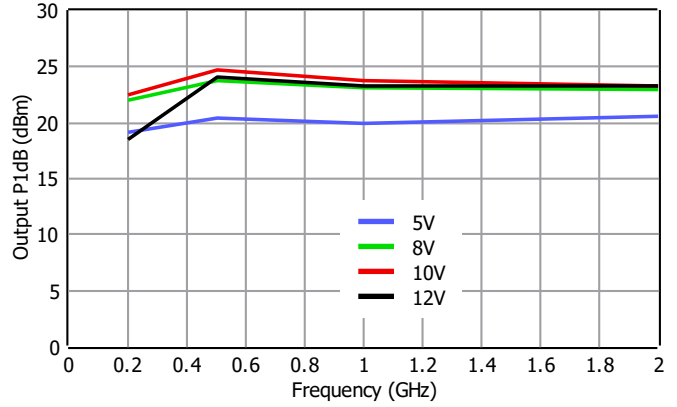
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

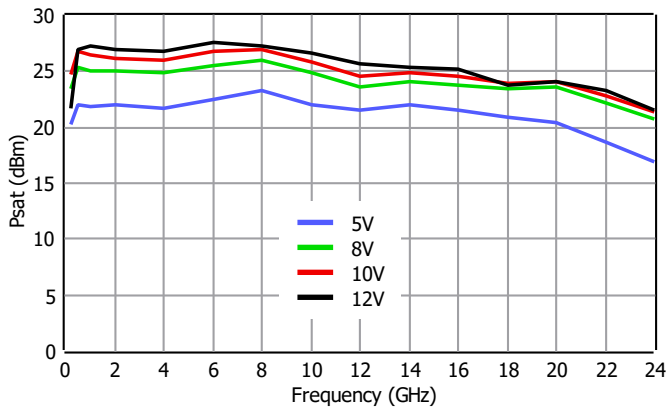
P1dB



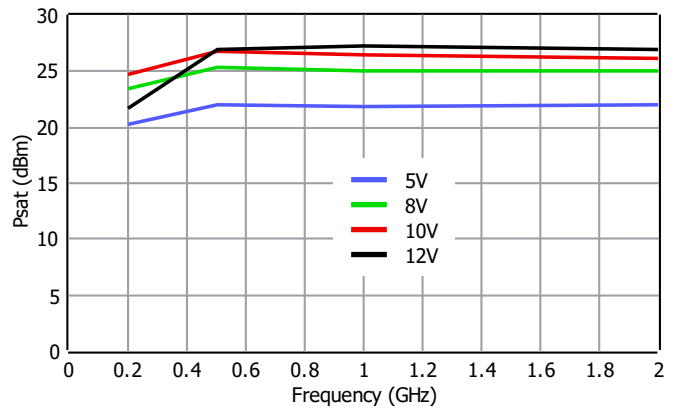
P1dB at Low Frequency



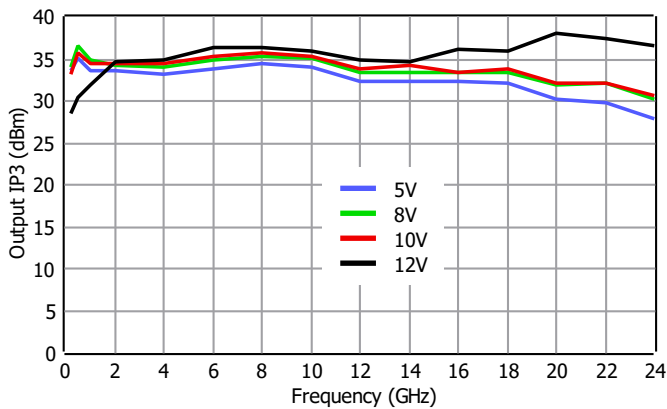
Psat



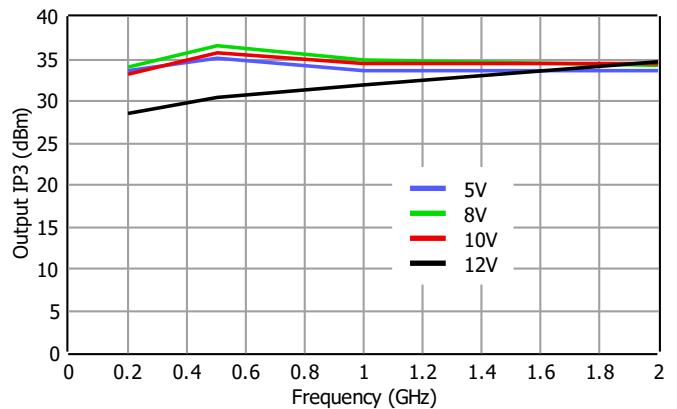
Psat at Low Frequency



IP3



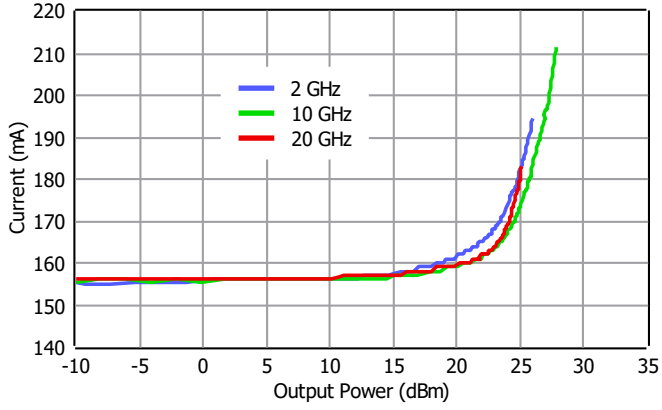
IP3 at Low Frequency



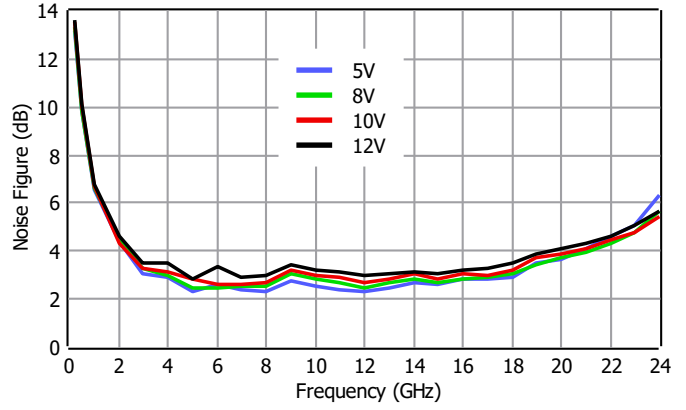
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

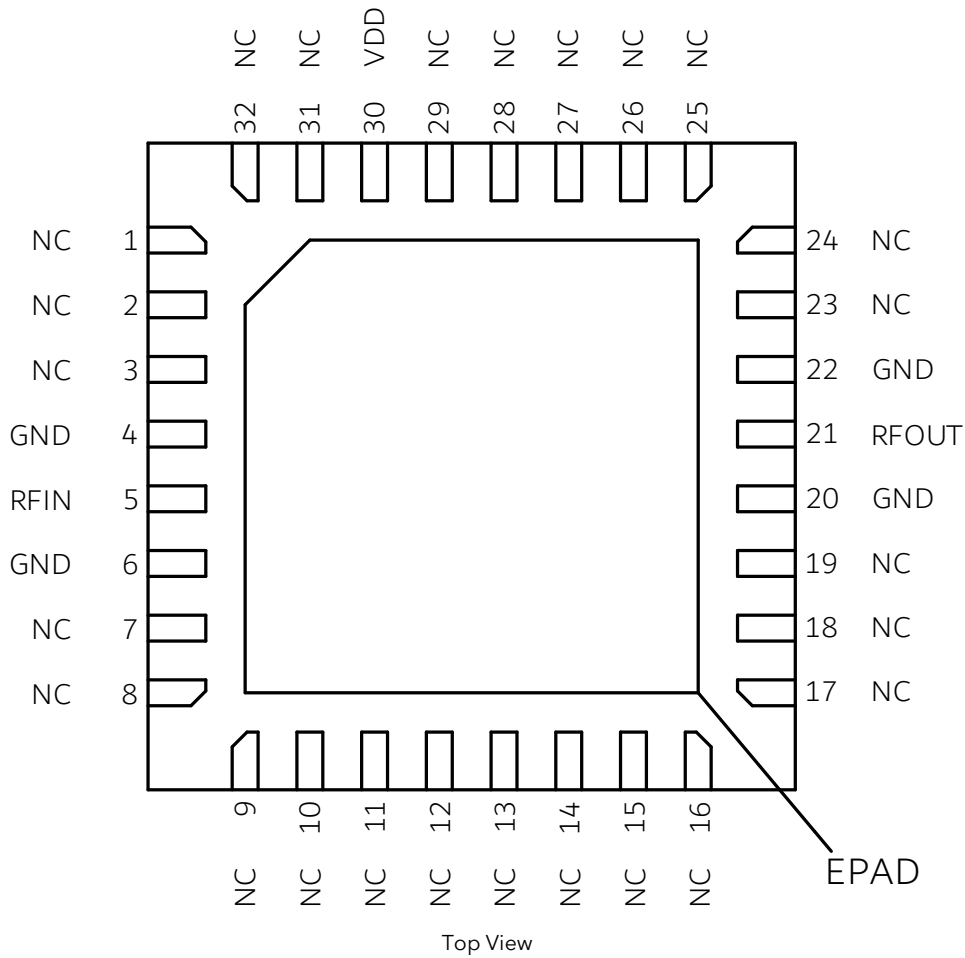
Output Power vs Current, Frequency



Noise Figure



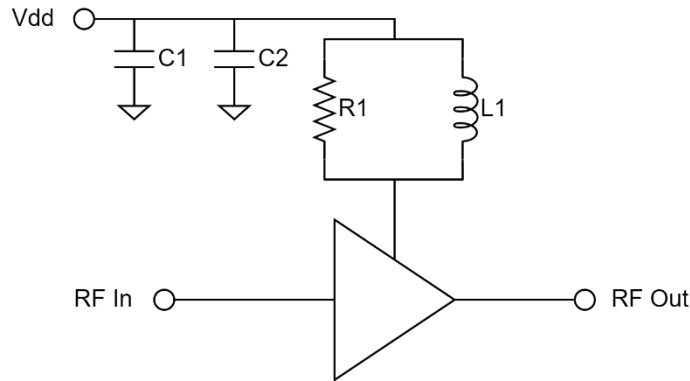
Pin Description



Pin Number	Pin Name	Description
5	RF IN	RF input pin. AC Coupled.
21	RF OUT	RF output pin. AC Coupled.
30	VDD	Vdd bias pin. Refer to Applications Information section for details.
1-3, 7-19, 23-29, 31, 32	NC	These pins are not internally connected. Can be grounded on the PCB.
4, 6, 20, 22	GND	Ground.
33	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Applications Information

Signal entering from RF IN goes to RF OUT with an amplification. Typical application schematic to operate the amplifier is given below.



The amplifier is optimized for simple biasing circuitry. It only requires low cost L1 and R1 for biasing. DC block capacitors and self-biasing circuitry are realized inside the MMIC. Contact for further information on L1 and R1.

C1 and C2 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 and C2 will improve this filtering. If this filtering is of no concern, then amplifier can be operated without C1 and C2.

Small signal data plots are gathered with probe PCB measurements to generate plots shown in this document.

Overtemperature small signal data plots are gathered with connectorized evaluation PCB measurements. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

Large signal and noise figure data are generated with connectorized evaluation PCB measurements. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

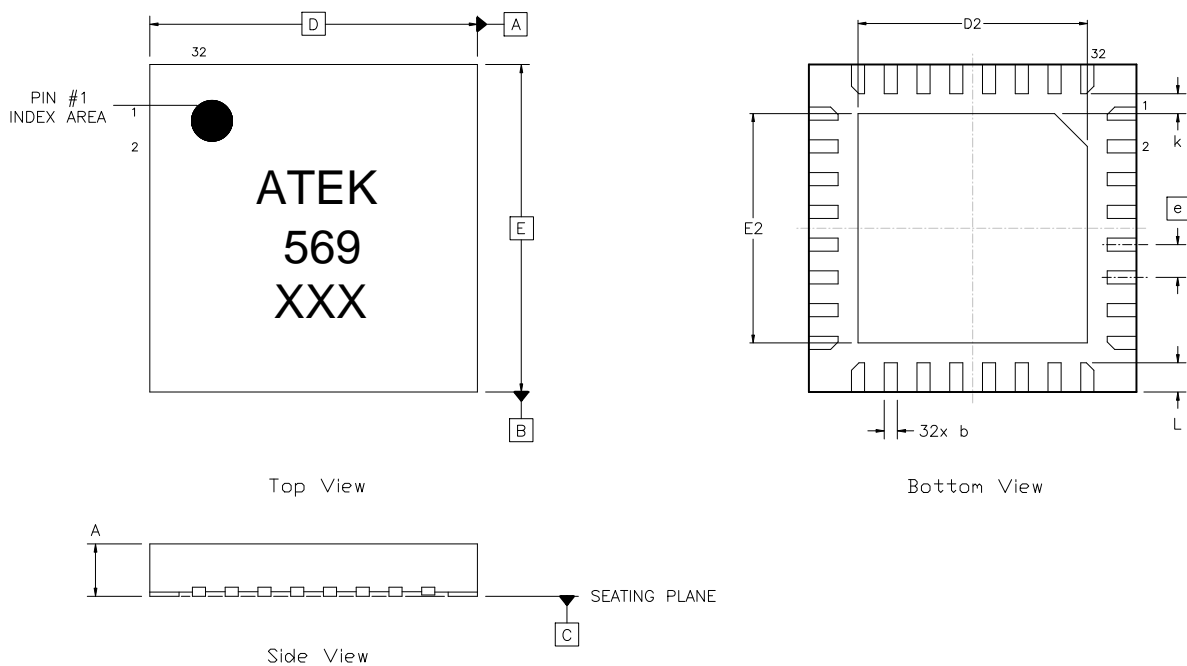
The NC pins of the Amplifier are connected to the GND on the PCBs used to generate the plots shown in this document.

Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	-55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information



NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	3.40	3.60
b	0.18	0.30	e	0.50	BSC
D	5.00	BSC	k	0.20	-
D2	3.40	3.60	L	0.40	0.50
E	5.00	BSC			

Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.

Web: www.atekmidas.com

Tel: +90-212-483-71-67

Email: support@atekmidas.com

Notice

This document and its contents are property of ATEK MIDAS. ATEK MIDAS has the right to change the document at any time without notice. ATEK MIDAS distributes this document as a service to its customers. ATEK MIDAS supports its customers to help them create market leader products. Customer is responsible from choosing the product and the configuration the product. This document is provided `as is` and does not provide any warranty.

Customer is responsible for the usage of this document, the information provided in the document and the usage of products. ATEK MIDAS shall have no responsibility from the customer products, customer applications and doings of customers.

Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	22.11.2024	Initial Release	
1.1	25.11.2024	Overttemperature Data Added	
1.2	28.11.2024	Format and Content Fixed	