

0.2 to 26 GHz Driver Amplifier

The ATEK569N5 is a GaAs PHEMT wideband distributed amplifier operating from 0.2 to 26GHz

The ATEK569N5 amplifier provides a flat gain of 14dB with an OIP3 of +35dBm and a +25dBm P1dB while operating from a single supply voltage of +10V drawing 190mA of current. The DC power bias of +5V to +12V can be supplied to the RF output port using an external bias-T.

The amplifier achieves a low noise figure of 3dB typical over the 6 to 18GHz band with +35dBm OIP3 enabling a high dynamic range driver amplifier application.

The driver Amplifier is housed in a compact 5x5 mm SMD package with input and output matched to 50 ohms internally.

Evaluation Board, bare die (ATEK569), custom package, and module options are available upon request.

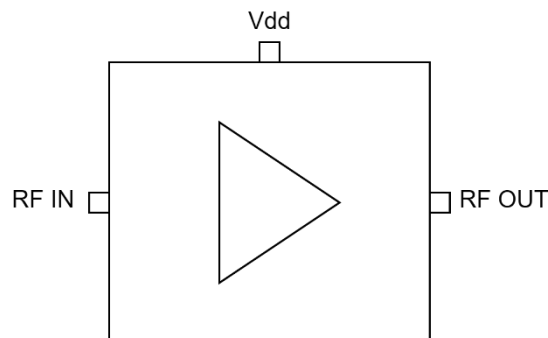
Product Features

- Frequency Range: 0.2 to 26 GHz
- Gain: 14 dB
- P1dB: +25.5 dBm
- IP3: +35 dBm
- Single Supply +5V to +12V
- On-chip DC Block Capacitors
- 5x5 mm compact size

Applications

- Wideband Receivers, SDRs
- Microwave Radio
- Test and Measurement
- EW / ECM / C-UAS
- Military and Commercial Radar

Functional Block Diagram



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Electrical Specifications

Conditions unless otherwise specified: $V_{DD} = 12\text{ V}$, Typical, $T = 25\text{ C}$, CW.

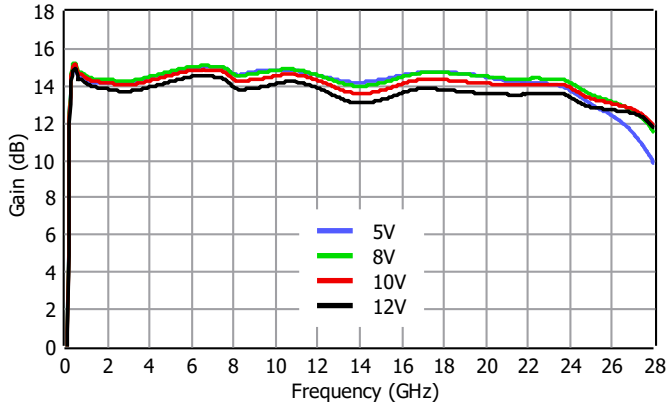
Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.2		26	GHz
Gain	0.25 GHz	11.6	13.6		dB
	2 GHz	11.8	13.8		
	8 GHz	11.9	13.9		
	12 GHz	11.8	13.8		
	18 GHz	11.8	13.8		
	26 GHz	10.7	12.7		
Isolation	0.25 GHz		64		dB
	2 GHz		60		
	8 GHz		45		
	12 GHz		40		
	18 GHz		33		
	26 GHz		28		
Input Return Loss			-14		dB
Output Return Loss			-13		dB
Noise Figure at 5V			3		dB
Output IP3			35		dBm
Output P1dB	0.2 - 1 GHz	19	23		dBm
	1 - 18 GHz	23	25.5		
	18 - 26 GHz	22	24.5		
Psat			27.5		dBm
DC Supply Voltage (Vdd)			10 12	10 12	V
DC Supply Current (Idd)			190 200	290 315	mA
Operating Temperature		-40		85	°C

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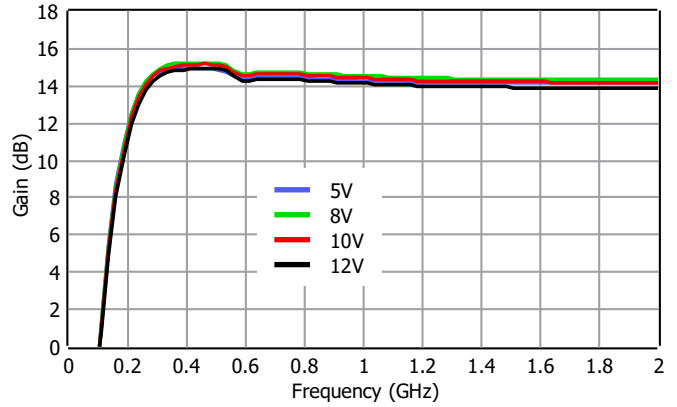
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

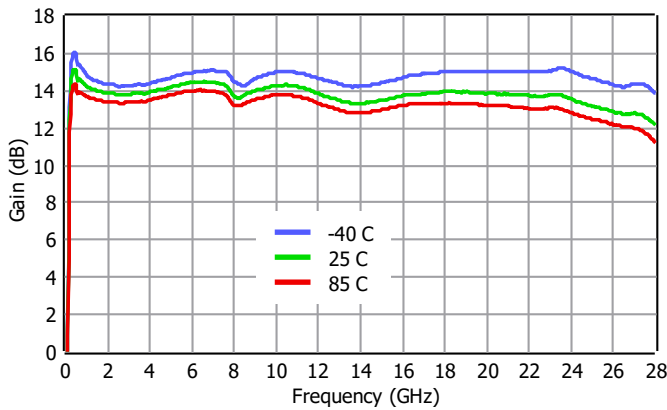
Gain



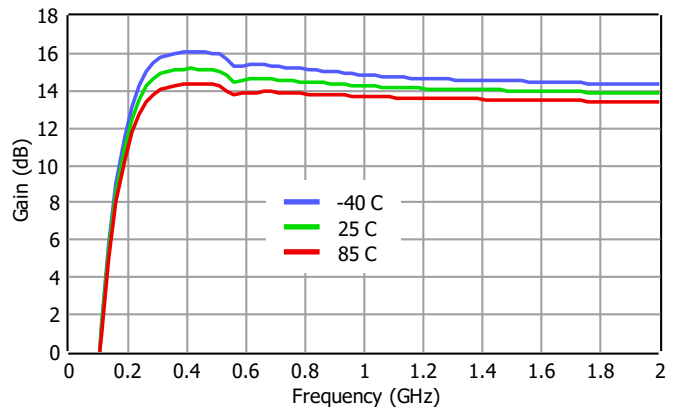
Gain at Low Frequency



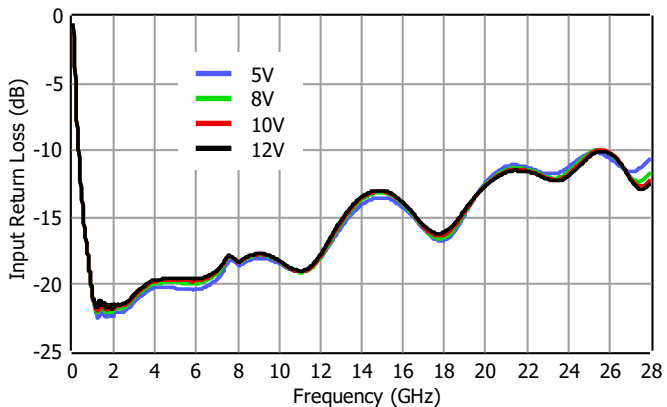
Gain vs Temperature



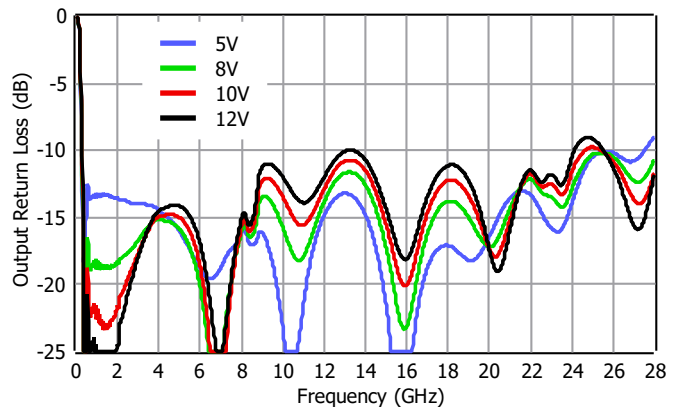
Gain vs Temperature at Low Frequency



Input Return Loss



Output Return Loss

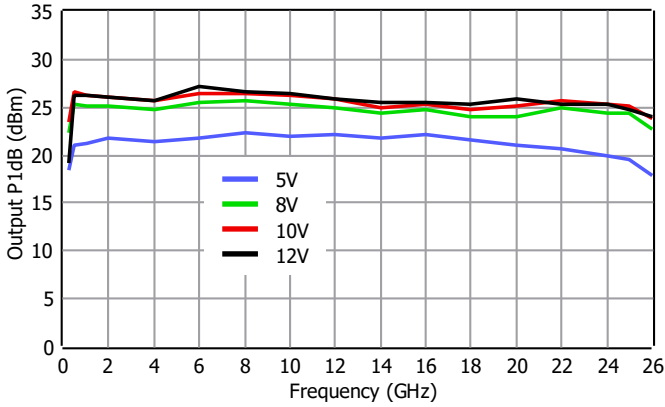


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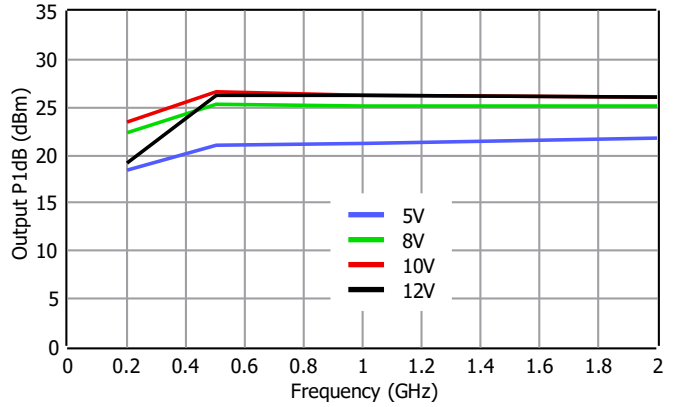
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

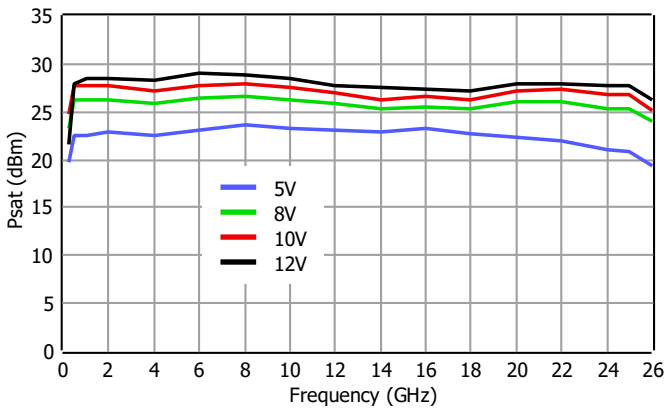
P1dB



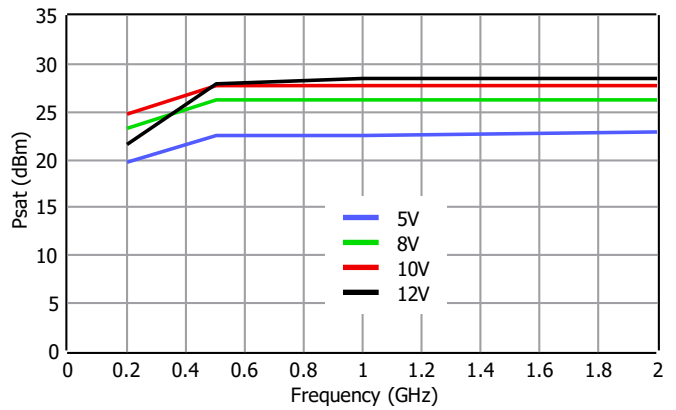
P1dB at Low Frequency



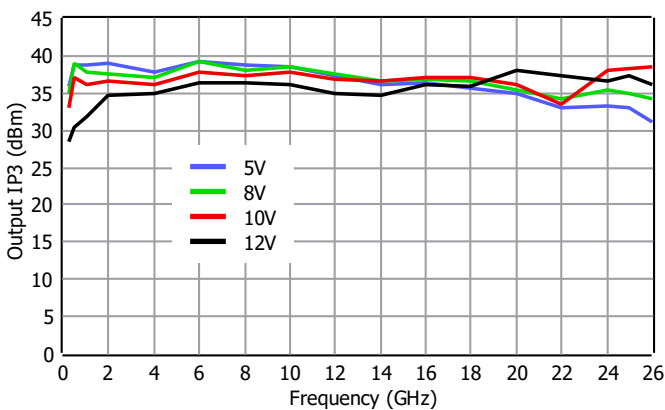
Psat



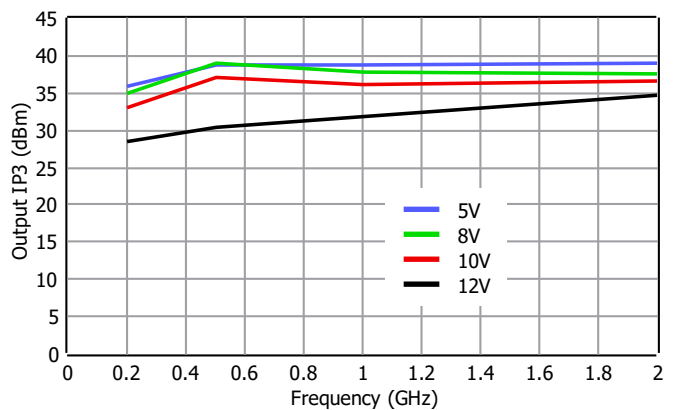
Psat at Low Frequency



IP3



IP3 at Low Frequency

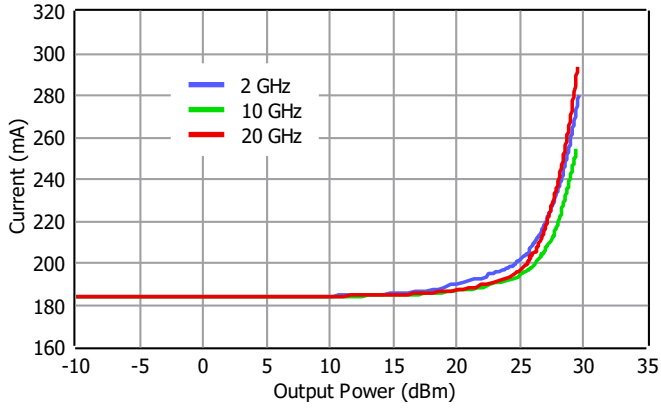


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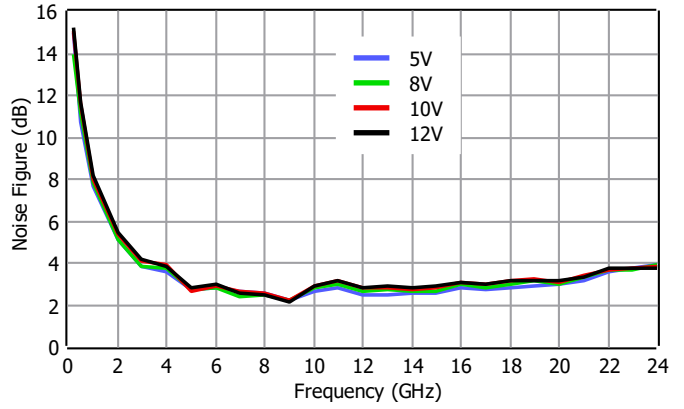
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 12V$, Typical, $T = 25\text{ C}$, CW.

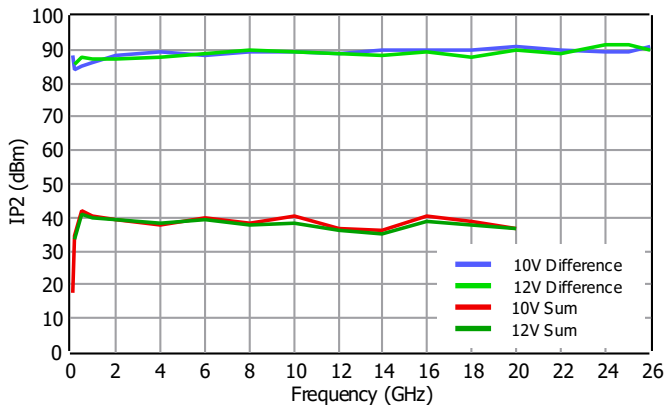
Output Power vs Current, Frequency



Noise Figure

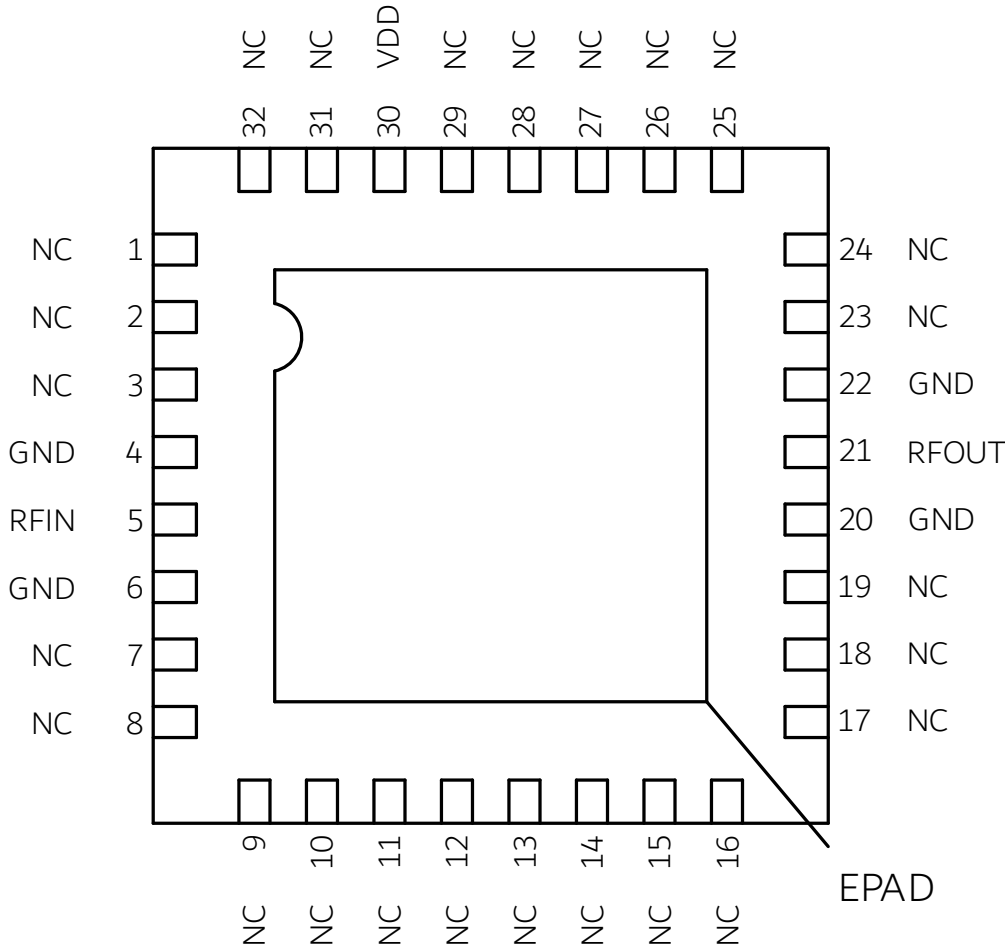


IP2 at Pout = 0dBm/tone



0.2 to 26 GHz Driver Amplifier

Pin Description

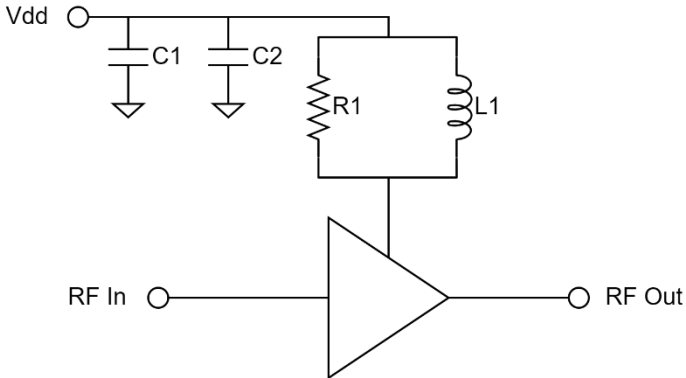


Pin Number	Pin Name	Description
5	RF IN	RF input pin. AC Coupled.
21	RF OUT	RF output pin. AC Coupled.
30	VDD	Vdd bias pin. Refer to Applications Information section for details.
1-3, 7-19, 23-29, 31, 32	NC	These pins are not internally connected. Can be grounded on the PCB.
4, 6, 20, 22	GND	Ground.
33	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

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Applications Information

Signal entering from RF IN goes to RF OUT with an amplification.
A typical application schematic to operate the amplifier is given below.



The amplifier is optimized for simple biasing circuitry. It only requires low cost L1 and R1 for biasing. DC block capacitors and self-biasing circuitry are realized inside the MMIC. Contact for further information on L1 and R1.

C1 and C2 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 and C2 will improve this filtering. If this filtering is of no concern, then the amplifier can be operated without C1 and C2.

Small signal data plots are gathered with probe PCB measurements to generate plots shown in this document.

Over temperature small signal data plots are gathered with the ATEK569N5 mounted to a connectorized evaluation board. The PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

Large signal and noise figure data are generated with connectorized evaluation of PCB measurements. Then the PCB trace and connector transition losses are de-embedded, to generate plots shown in this document.

The NC pins of the Amplifier are connected to the GND on the PCBs used to generate the plots shown in this document.

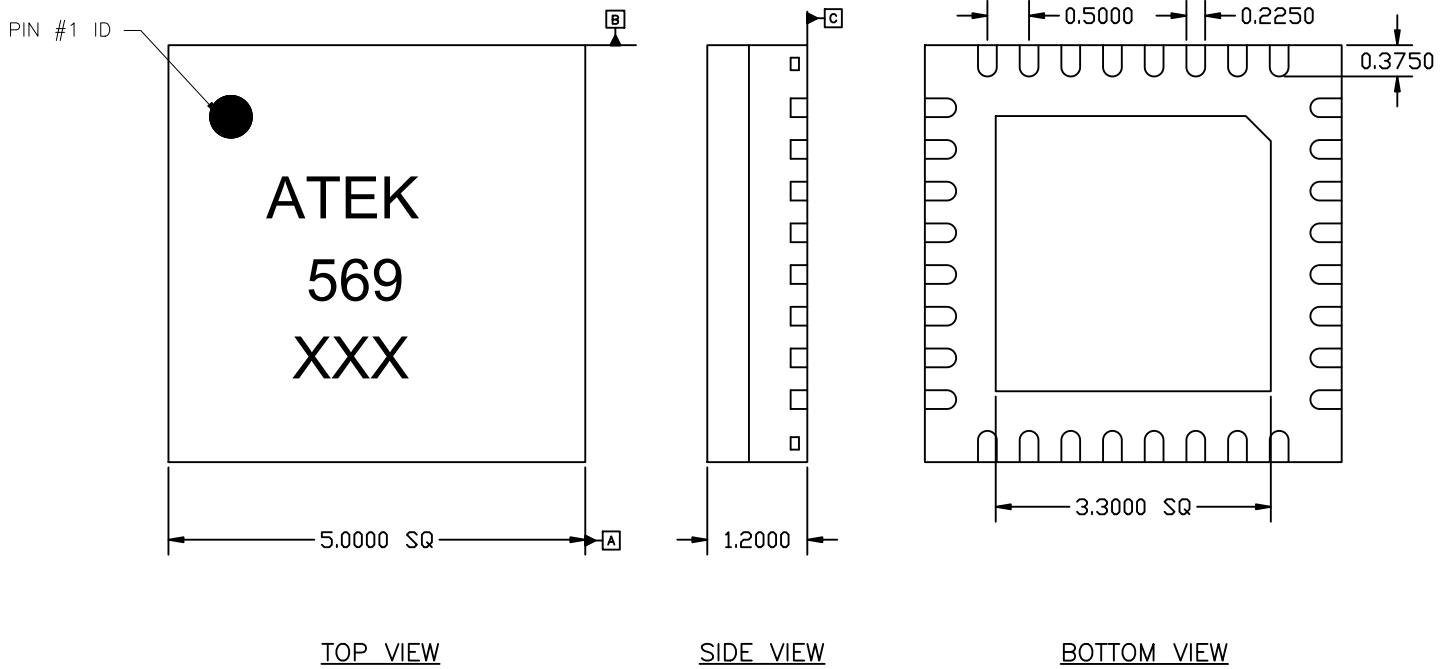
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Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltage (Vdd)	+12.5 V
RF Input Power (Vdd = +10.0V)	+25 dBm
Channel Temperature	+175 °C
Power Dissipation (Ta=85 °C)	3.79 W
Thermal Resistance	24 °C/W
Storage Temperature	-55 to +125°C
Operating Temperature	-40 to +85°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information



NOTES

1. ALL DIMENSIONS IN MM
2. MARKING XXX INDICATES INTERNAL LOT CODE

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Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.

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Email: support@atekmidas.com

Notice

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	22.11.2024	Initial Release	
1.1	25.11.2024	Overtemperature Data Added	
1.2	28.11.2024	Format and Content Fixed	
1.3	14.01.2024	Mechanical and Marking Information Revised	
1.4	06.02.2026	Electrical Specifications AMR Table and Mechanical and Marking Information Revised	
1.5	30.03.2026	Plots Added	
1.6	06.06.2026	Updated Format	