Product Description

ATEK357P4 is a wideband 5-bit Digital Step Attenuator with 30 dB attenuation range. Attenuator frequency of operation goes down to Low Frequency close to DC and goes up to 20 GHz.

Bias and control voltages of the attenuator are positive, which eliminates the need for negative voltage rails.

Attenuator is housed in compact 4x4 mm low cost SMD package, input and outputs are matched to 50 ohms internally.

Evaluation Board, bare die, custom package, and module options are available upon request.

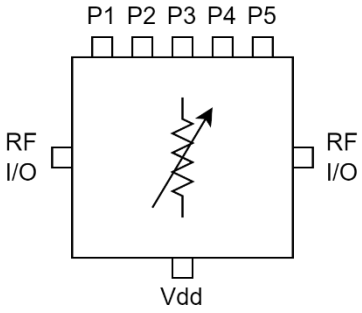
Product Features

- Frequency Range: LF - 20 GHz
- Insertion Loss: 3.9 dB at 10 GHz
- Attenuation Range: 31 dB
- Input IP3: 43 dBm
- Positive Supply
- Positive Control
- 4x4 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test Equipment
- Radar
- Electronic Warfare

Functional Block Diagram



Electrical Specifications

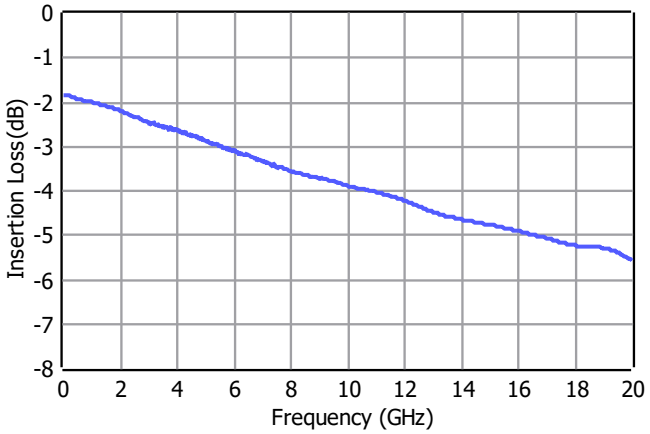
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		20	GHz
Insertion Loss	0.01 GHz		2		dB
	2 GHz		2.5		
	8 GHz		3.5		
	14 GHz		4.6		
	20 GHz		5.6		
Attenuation Range	0.01 GHz		31		dB
	2 GHz		30.5		
	8 GHz		30		
	14 GHz		30.5		
	20 GHz		29.5		
State Error			0.7		dB
Input Return Loss			-13		dB
Output Return Loss			-14		dB
Input P1dB			27		dBm
Input IP3			43		dBm
Switching Time (50% Vctrl to 90% of RF Output)			58		ns
DC Supply Voltage (Vdd)			5		V
DC Supply Current			5.5		mA
Control Voltage (P1–5)	Low		0		V
	High		5		
Operating Temperature		-40		85	°C

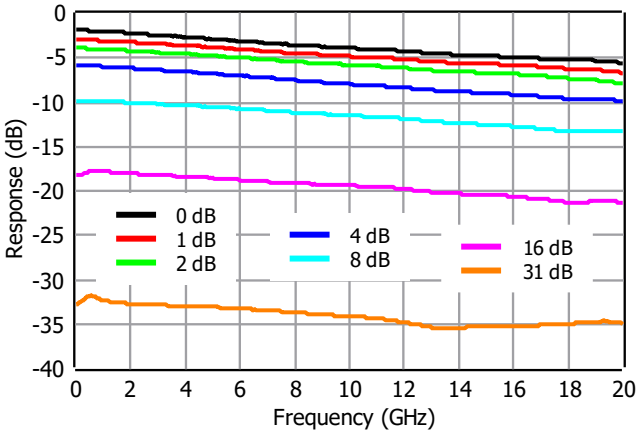
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

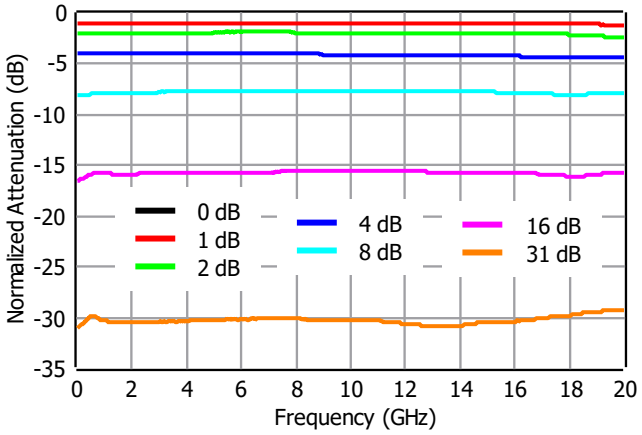
Insertion Loss



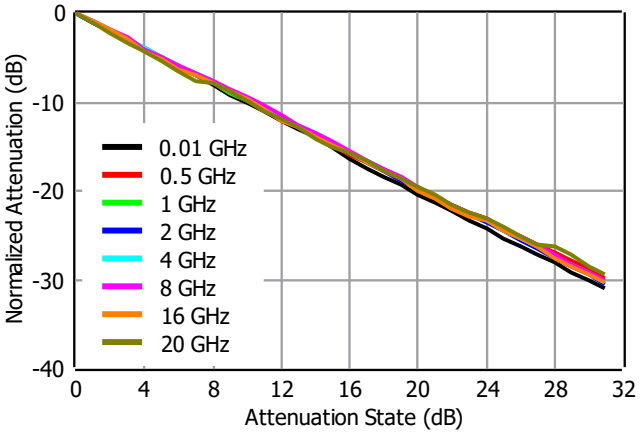
Insertion Loss vs. Attenuation State



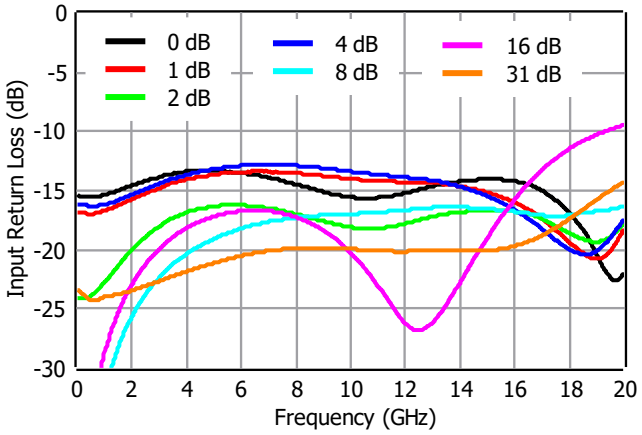
Normalized Attenuation



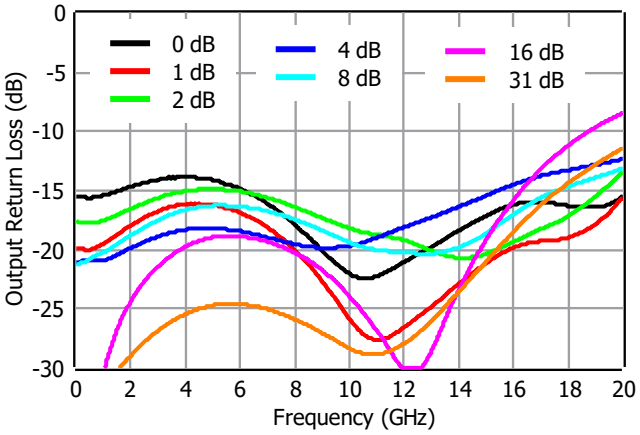
Normalized Attenuation vs. Attenuation State, Frequency



Input Return Loss



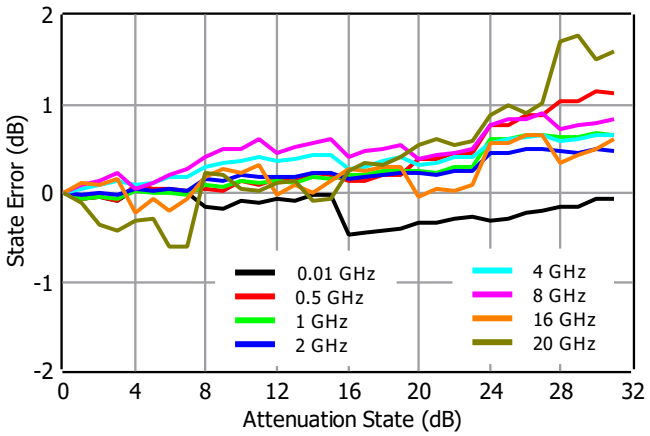
Output Return Loss



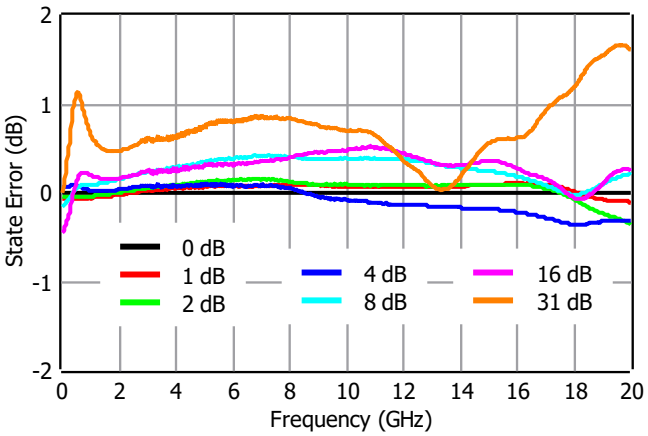
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

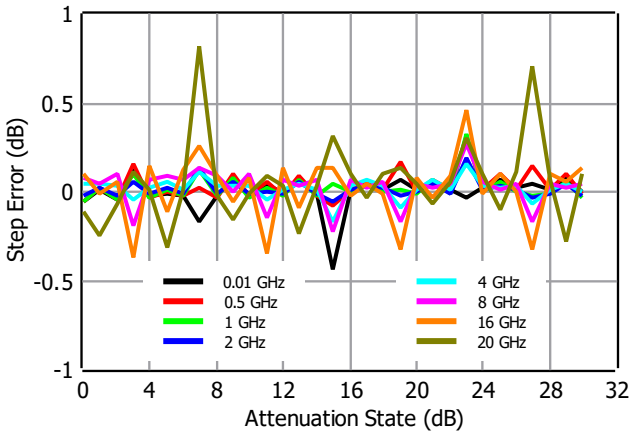
State Error vs. Attenuation State, Frequency



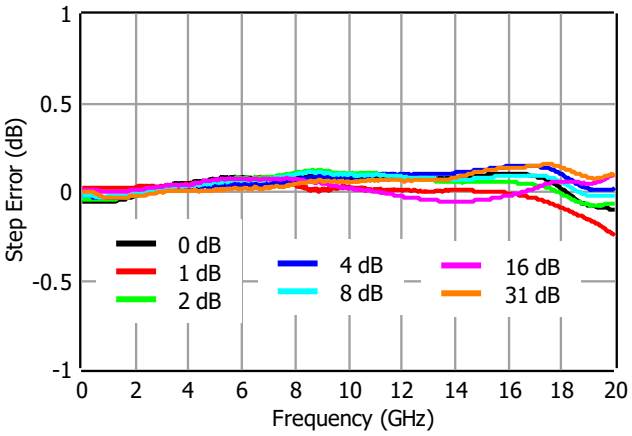
State Error vs. Attenuation State



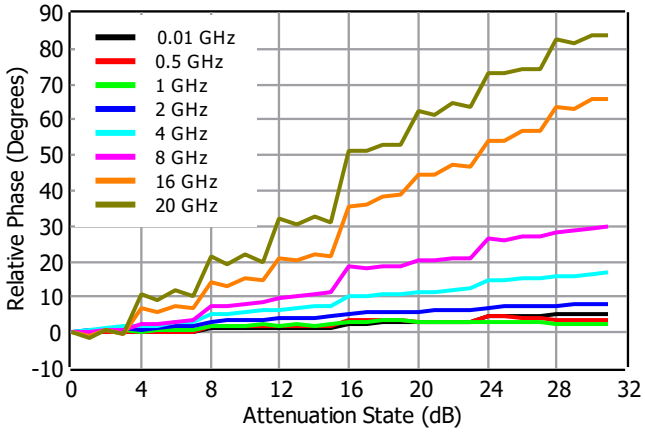
Step Error vs Attenuation State, Frequency



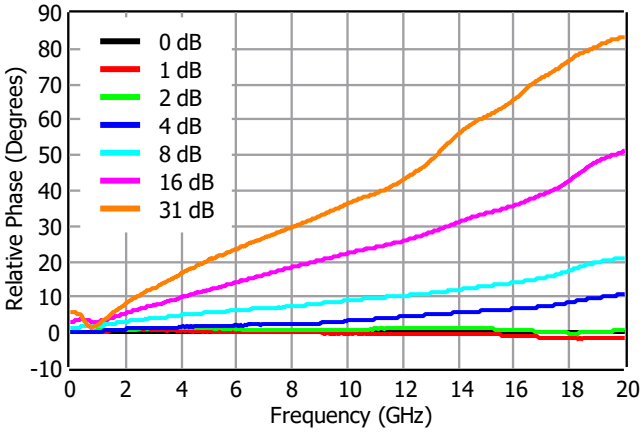
Step Error vs. Attenuation State



Relative Phase vs. Attenuation State, Frequency



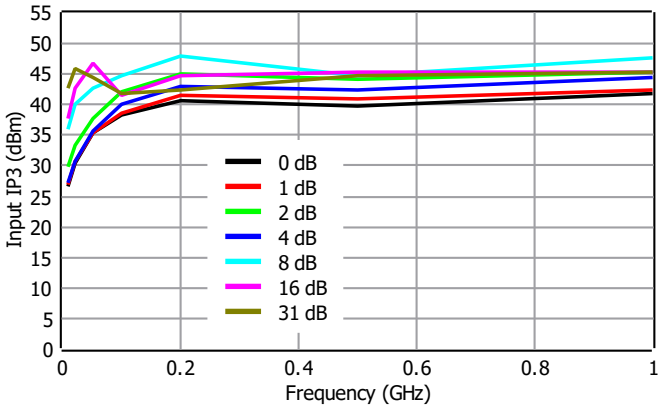
Relative Phase vs. Attenuation State



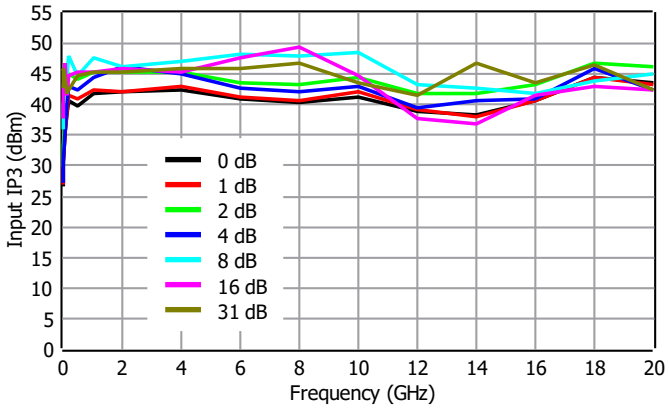
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

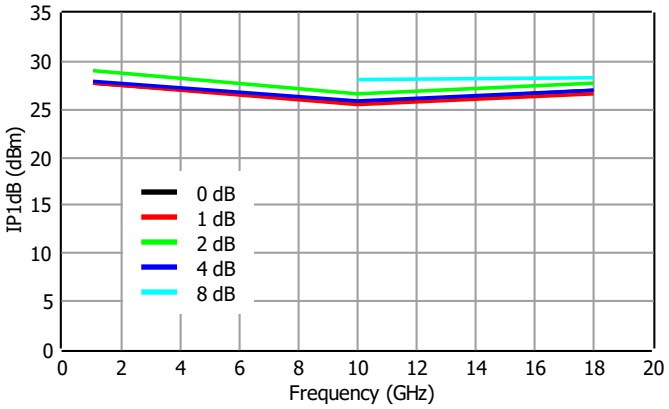
Input IP3 at Low Frequency



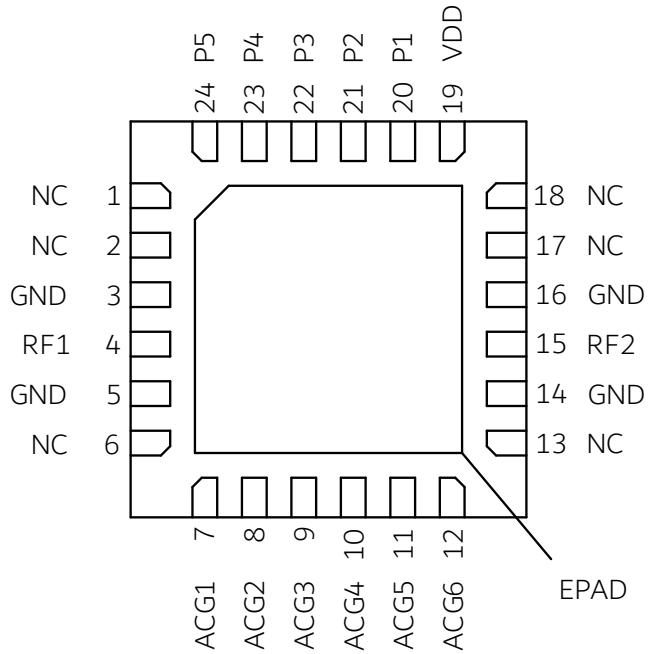
Input IP3



Input P1dB



Pin Description



Pin Number	Pin Name	Description
4	RF1	RF input/output pin. Wideband DC block capacitor is required.
15	RF2	RF input/output pin. Wideband DC block capacitor is required.
19	VDD	Vdd bias pin.
20	P1	Control voltage pin for parallel control interface.
21	P2	Control voltage pin for parallel control interface.
22	P3	Control voltage pin for parallel control interface.
23	P4	Control voltage pin for parallel control interface.
24	P5	Control voltage pin for parallel control interface.
7	ACG1	AC ground pin. External shunt capacitor is required.
8	ACG2	AC ground pin. External shunt capacitor is required.
9	ACG3	AC ground pin. External shunt capacitor is required.
10	ACG4	AC ground pin. External shunt capacitor is required.
11	ACG5	AC ground pin. External shunt capacitor is required.
12	ACG6	AC ground pin. External shunt capacitor is required.
1, 2, 6, 13, 17, 18	NC	These pins are not internally connected. Can be grounded on the PCB.
3, 5, 14, 16	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

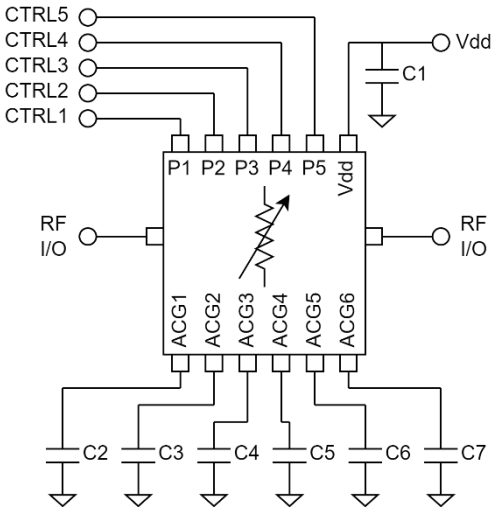
P5	P4	P3	P2	P1	Attenuation State
LOW	LOW	LOW	LOW	LOW	0 dB
LOW	LOW	LOW	LOW	HIGH	1 dB
LOW	LOW	LOW	HIGH	LOW	2 dB
LOW	LOW	HIGH	LOW	LOW	4 dB
LOW	HIGH	LOW	LOW	LOW	8 dB
HIGH	LOW	LOW	LOW	LOW	16 dB
HIGH	HIGH	HIGH	HIGH	HIGH	31 dB

Applications Information

Signal entering from RF IN goes to RF OUT with an attenuation level set by control pins.

Vdd bias is 5 V and control voltages are CMOS compatible. Attenuation level can be set by switching control voltages between 0 V to 5 V. Operating the attenuator is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the attenuator is given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then attenuator can be operated without C1.

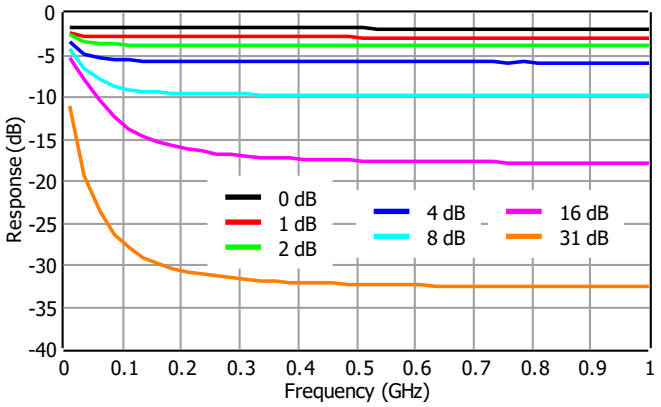
If needed, to filter out the ripples and unwanted signals on the external CTRL1 to CTRL5 signal, a low pass filter in series R, shunt C configuration can be implemented on the CTRL1 to CTRL5 line. Note that external RC filtering limits the attenuation switching speed of the attenuator.

C2, C3, C4, C5, C6 and C7 are AC ground capacitors. Values of these capacitors should be chosen considering the lowest operation frequency of the application. 100 nF is used for ACG capacitors to generate the measurement results in this document.
When ACG capacitorss are not used, low frequency performance will degrade, but the part still can operate down to 250 MHz. Typical performance plots without ACG capacitors are below.

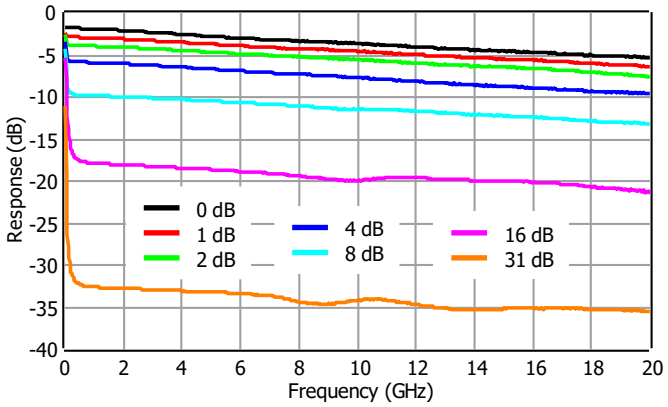
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Insertion Loss vs. Attenuation State at Low Frequency



Insertion Loss vs. Attenuation State



CTRL1 to CTRL5 voltages are used for setting the attenuation level.

All measurement results presented on this document are taken with a set-up, where RF1 is an input and RF2 is an output.

For the higher states of Input P1dB measurement, Input P1dB is more than the shown states. These states could not measure due to setup limits.

Large signal datasheet plots are generated by connectorized evaluation boards (EVBs), PCB and connector losses are de-embedded. Small signal plots are generated by probing the RF lines with RF probes to eliminate the connector transition effects.

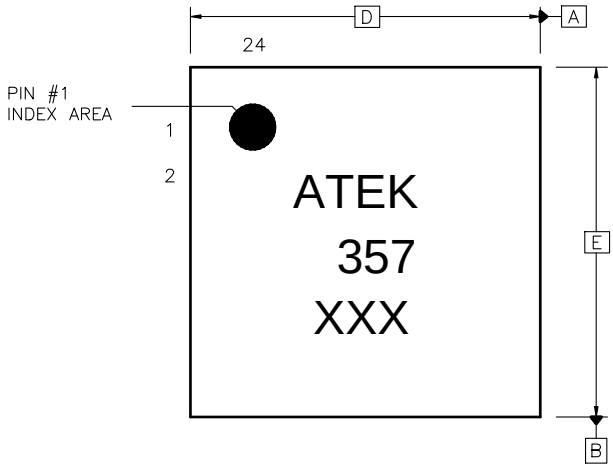
The NC pins of the attenuator are connected to the GND on the PCB used to generate the plots shown in this document.

Absolute Maximum Ratings

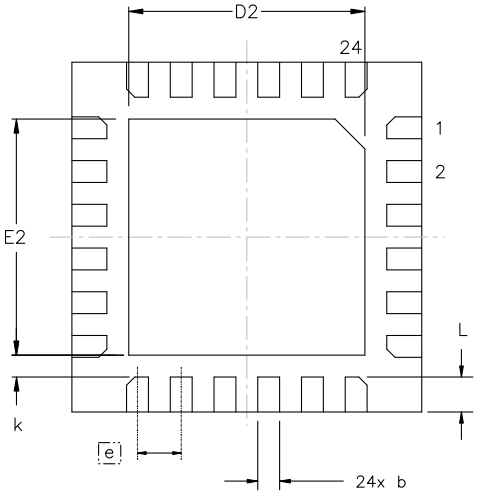
Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

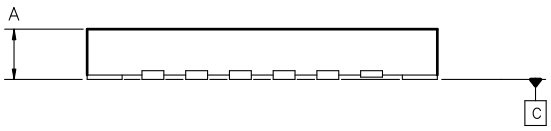
Mechanical and Marking Information



Top View



Bottom View



Side View

NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
b	0.18	0.30	e	0.50 BSC	
D	4.00 BSC		k	0.20	–
D2	2.60	2.80	L	0.35	0.45
E	4.00 BSC				

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

Notice

This document and its contents are property of ATEK MIDAS. ATEK MIDAS has the right to change the document at any time without notice. ATEK MIDAS distributes this document as a service to its customers. ATEK MIDAS supports its customers to help them create market leader products. Customer is responsible from choosing the product and the configuration the product. This document is provided `as is` and does not provide any warranty.
Customer is responsible for the usage of this document, the information provided in the document and the usage of products. ATEK MIDAS shall have no responsibility from the customer products, customer applications and doings of customers.

Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	21.03.2022	Initial Release	
1.1	16.04.2022	Design Revised	
1.2	01.10.2022	Application Notes Revised	
1.3	15.07.2023	Large Signal Data Added	
1.4	24.04.2024	Large Signal Data Added	
1.5	16.09.2024	Application Section Updated	
1.6	17.09.2024	Switching Time Data Added	