Product Description

ATEK260AP3 is a wideband absorptive SPDT switch with low loss and high isolation. Frequency of operation starts from low frequencies close to DC, goes up to 6 GHz. Usable bandwidth covers 7 GHz.

Operating from positive supply voltage and switch state is chosen by positive voltage control interface. Eliminates the need for external negative bias circuitry for the user.

RF input outputs are matched to 50 ohms internally. Switch is housed in a compact low cost 3x3 mm surface mount package.

Evaluation Board, bare die, custom package, and module options are available upon request.

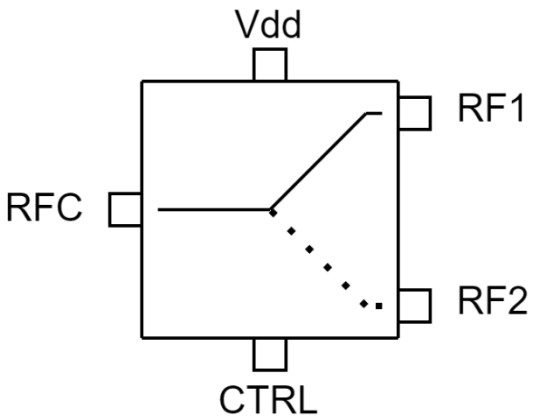
Product Features

- Frequency Range: LF - 6 GHz
- Insertion Loss: 0.6 dB
- Positive Supply
- Positive Control
- 3x3 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test and Measurement
- SATCOM
- SDR

Functional Block Diagram



Electrical Specifications

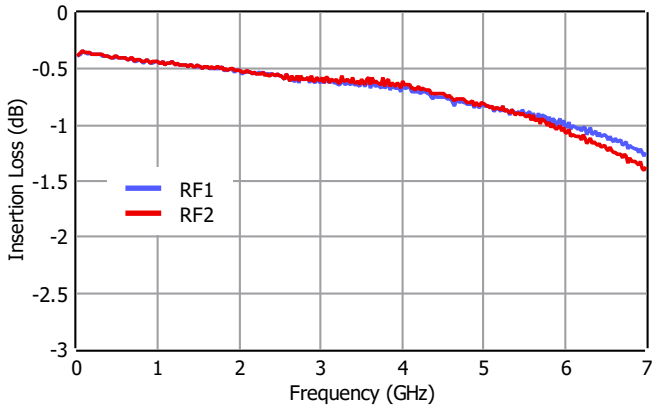
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		6	GHz
Insertion Loss	0.5 GHz		0.4		dB
	1 GHz		0.45		
	2 GHz		0.5		
	4 GHz		0.65		
	6 GHz		1		
Isolation	0.5 GHz		53		dB
	1 GHz		47		
	2 GHz		41		
	4 GHz		35		
	6 GHz		30		
Input Return Loss			-16		dB
Output Return Loss			-16		dB
Input IP3			47		dBm
Input P1dB			TBD		dBm
Switching Speed	On		95		ns
	Off		50		
DC Supply Voltage (Vdd)		3	5	5.5	V
DC Supply Current			1		mA
Control Level	Low	-0.1		0.5	V
	High	3		5	
Operating Temperature		-40		85	°C

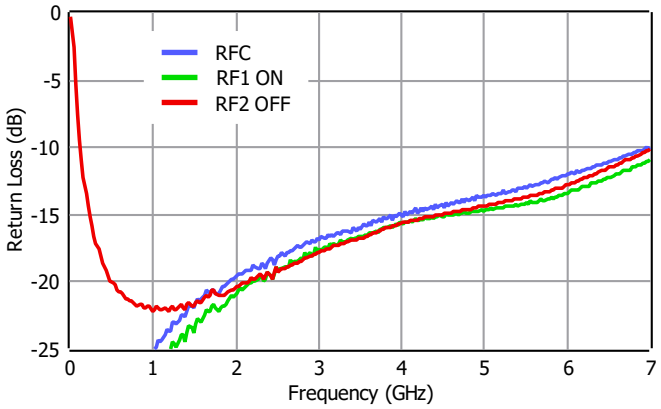
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C.

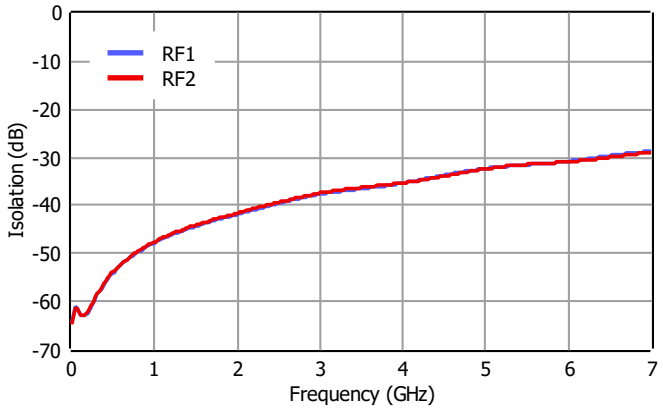
Insertion Loss



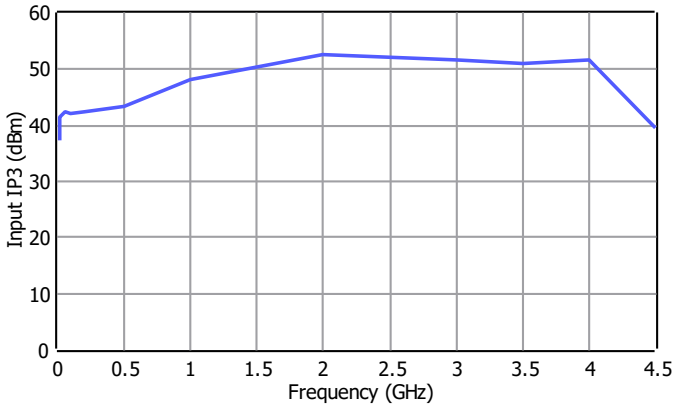
Return Loss



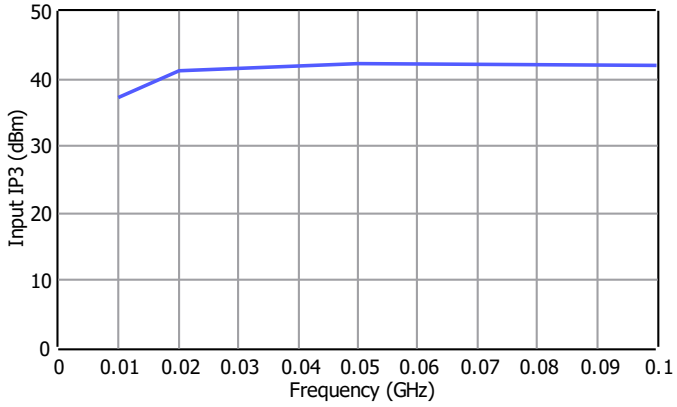
Isolation from RFC to RF1 and RF2



Input IP3



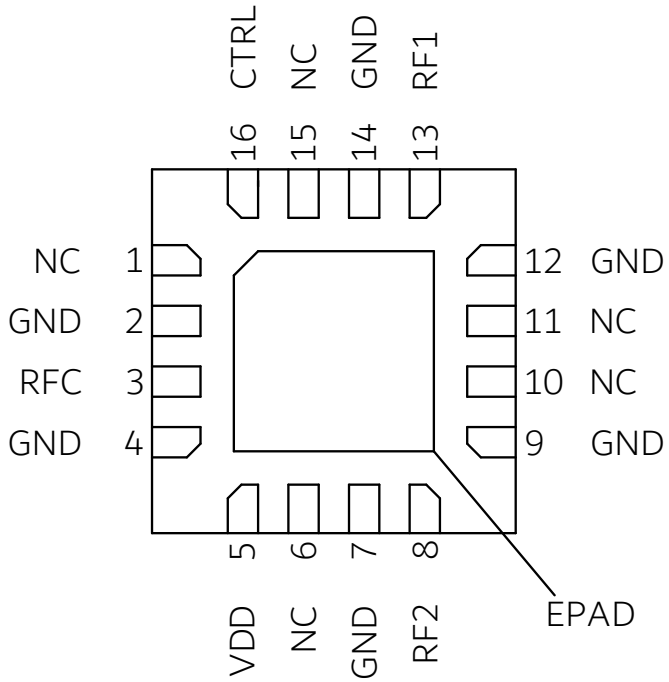
Input IP3 at Low Frequencies



Input P1dB

TBD

Pin Description



Top View

Pin Number	Pin Name	Description
3	RFC	RF input/output pin. Wideband external DC block capacitor is required.
13	RF1	RF input/output pin. Wideband external DC block capacitor is required.
8	RF2	RF input/output pin. Wideband external DC block capacitor is required.
5	VDD	Vdd bias pin.
16	CTRL	Control pin.
1, 6, 10, 11, 15	NC	These pins are not internally connected. Can be grounded on the PCB.
2, 4, 7, 9, 12, 14	GND	Ground.
17	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

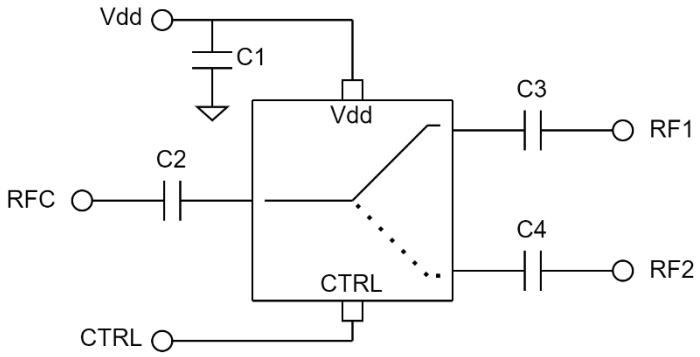
CTRL	RFC to RF1	RFC to RF2
HIGH	ON	OFF
LOW	OFF	ON

Applications Information

Signal entering from RFC goes to RF1 or RF2 depending on the switch state set by the user.

Vdd bias is 5 V and control voltages are CMOS compatible. Switch state can be set by switching control voltages between 0 V to 5 V. Operating the switch is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the SPDT switch given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then SPDT can be operated without C1.

C2, C3 and C4 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss.

If needed, to filter out the ripples and unwanted signals on the external CTRL signal, a low pass filter in series R, shunt C configuration can be implemented on the CTRL line. Note that external RC filtering limits the state switching speed of the SPDT.

CTRL voltage is used for setting the switch state.

All datasheet plots are generated by an evaluation board (EVB) with the application schematic provided above. RF lines on the EVB are connected to the RF pins of the SPDT. PCB and connector losses are de-embedded.

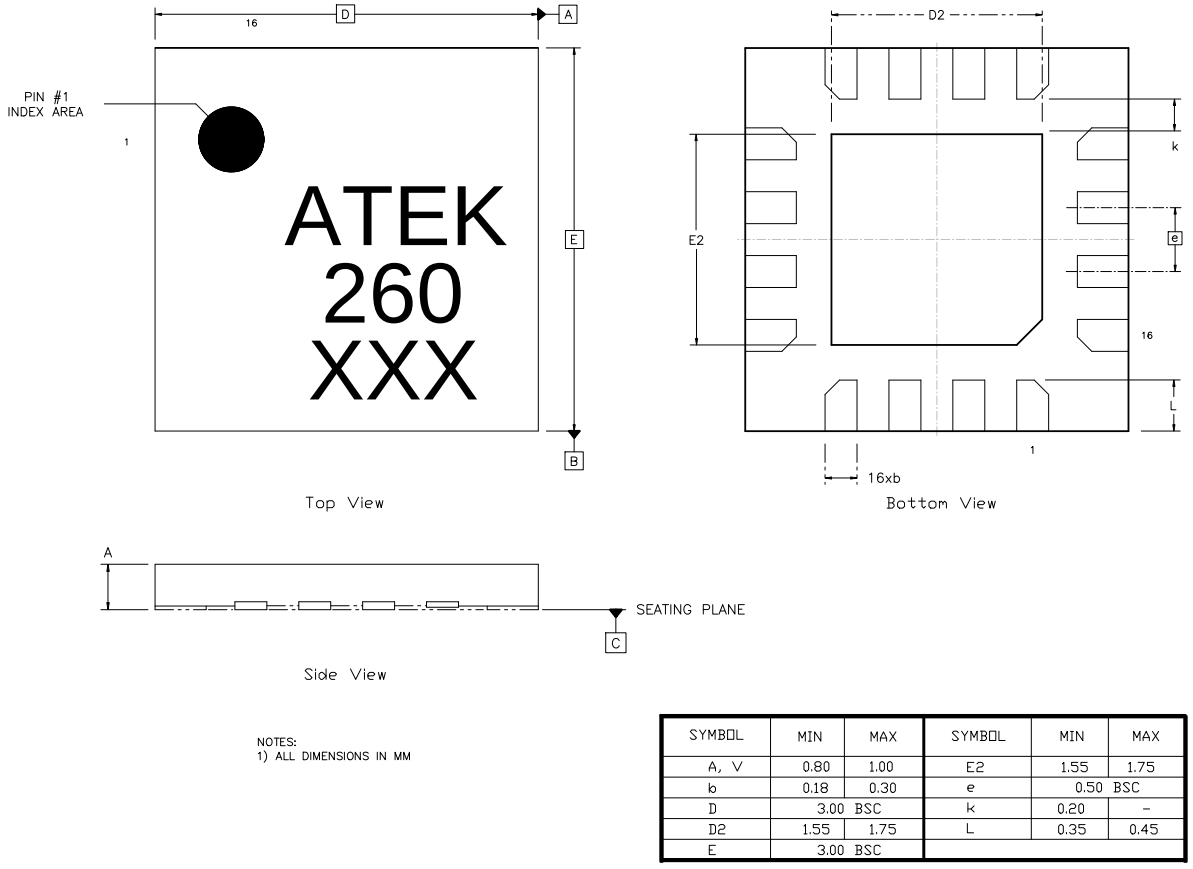
NC pins of the SPDT are connected to the GND on the EVB used to generate the plots shown in this document.

Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information



NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	1.55	1.75
b	0.18	0.30	e	0.50 BSC	
D	3.00 BSC		k	0.20	–
D2	1.55	1.75	L	0.35	0.45
E	3.00 BSC				

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	25.10.2023	Initial Release	
1.1	12.01.2024	Plots Revised	