Product Description

ATEK257P4 is a wideband reflective SP4T switch with low loss and high isolation. Frequency of operation starts from low frequencies close to DC, goes up to 16 GHz.

Operating from positive supply voltage and switch state is chosen by positive voltage control interface. Eliminates the need for external negative bias circuitry for the user.

RF input outputs are matched to 50 ohms internally. Switch is housed in a compact low cost 4x4 mm surface mount package.

Evaluation Board, bare die, custom package, and module options are available upon request.

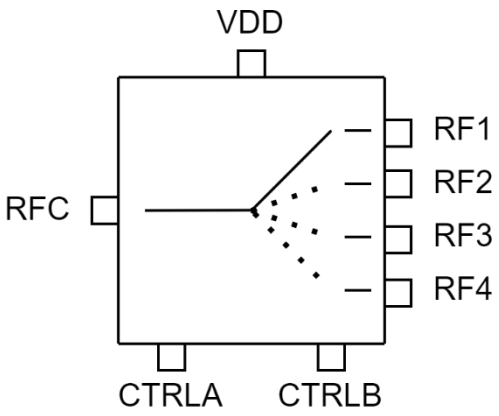
Product Features

- Frequency Range: LF - 16 GHz
- Insertion Loss: 2.4 dB at 10 GHz
- Positive Supply
- Positive Control
- 4x4 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test Equipment
- SDR

Functional Block Diagram



Electrical Specifications

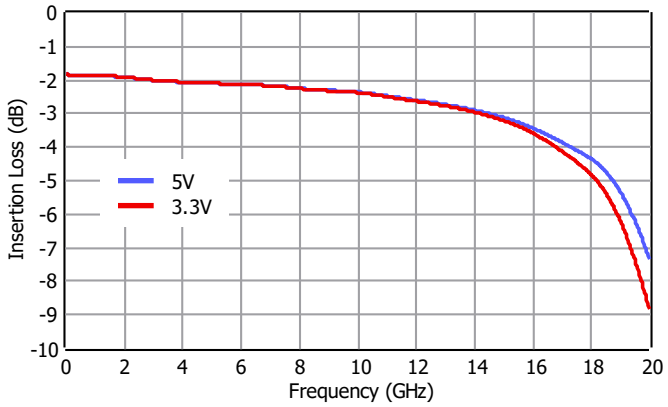
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		16	GHz
Insertion Loss	2 GHz		1.9		dB
	4 GHz		2.1		
	8 GHz		2.3		
	12 GHz		2.6		
	16 GHz		3.5		
Isolation	2 GHz		56		dB
	4 GHz		48		
	8 GHz		40		
	12 GHz		35		
	16 GHz		30		
Input Return Loss			-13		dB
Output Return Loss			-16		dB
Input P1dB			TBD		dBm
Input IP3			TBD		dBm
Switching Time	On		TBD		ns
	Off		TBD		
DC Supply Voltage (Vdd)			5		V
DC Supply Current			2.8		mA
Control Voltage (CTRLA, CTRLB)	Low		0		V
	High		Vdd		
Operating Temperature		-40		85	°C

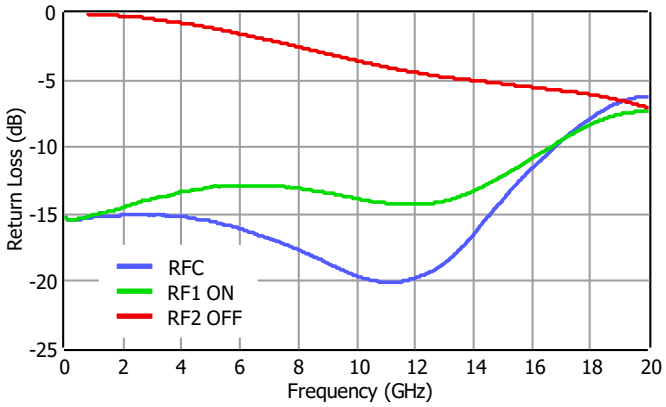
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

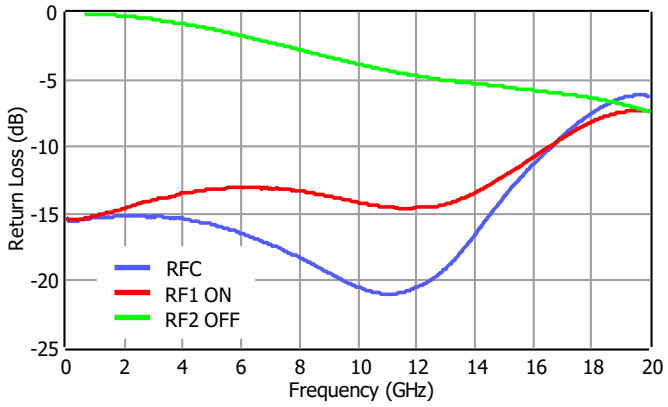
Insertion Loss



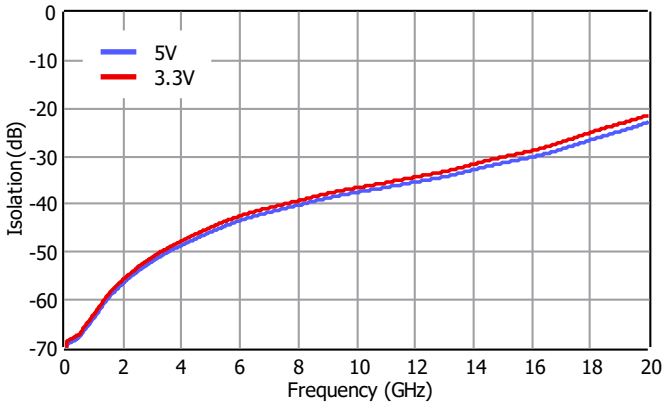
Return Loss at 5V



Return Loss at 3.3V



Isolation



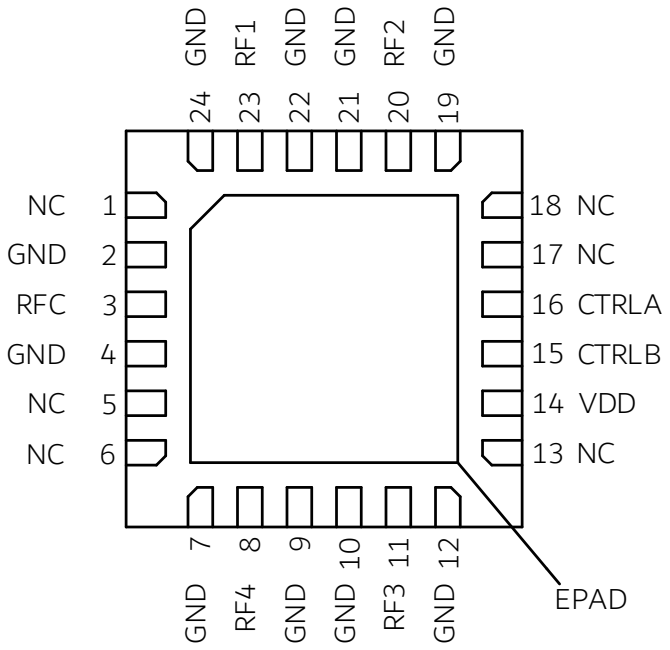
IIP3

TBD

IP1dB

TBD

Pin Description



Top View

Pin Number	Pin Name	Description
3	RFC	RF input/output pin. Wideband DC block capacitor is required.
23	RF1	RF input/output pin. Wideband DC block capacitor is required.
20	RF2	RF input/output pin. Wideband DC block capacitor is required.
11	RF3	RF input/output pin. Wideband DC block capacitor is required.
8	RF4	RF input/output pin. Wideband DC block capacitor is required.
14	VDD	Vdd bias pin.
16	CTRLA	Control pin.
15	CTRLB	Control pin
1, 5, 6, 13, 17, 18	NC	These pins are not internally connected. Can be grounded on the PCB.
2, 4, 7, 9, 10, 12, 19, 21, 22, 24	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

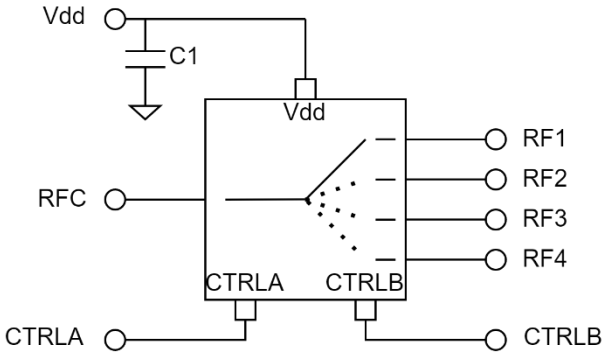
Control Interface

CTRLA	CTRLB	RFC to State
LOW	LOW	RF1
LOW	HIGH	RF2
HIGH	LOW	RF3
HIGH	HIGH	RF4

Applications Information

Signal entering from RFC goes to RF1-RF4 depending on the switch state set by the user.
Vdd bias is 5 V and control voltages are CMOS compatible. Switch state can be set by switching control voltages between 0 V to 5 V. Operating the switch is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the SP4T switch given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then SP4T can be operated without C1.

If needed, to filter out the ripples and unwanted signals on the external CTRL signals, a low pass filter in series R, shunt C configuration can be implemented on the CTRL lines. Note that external RC filtering limits the state switching speed of the SP4T.

CTRLA and CTRLB voltages are used for setting the switch state.

Small signal performance is measured with Probe PCB.
P1dB and IP3 performance is measured with connectorized evaluation PCB. Then the loss of the PCB is de-embedded to generate the data presented in this document.

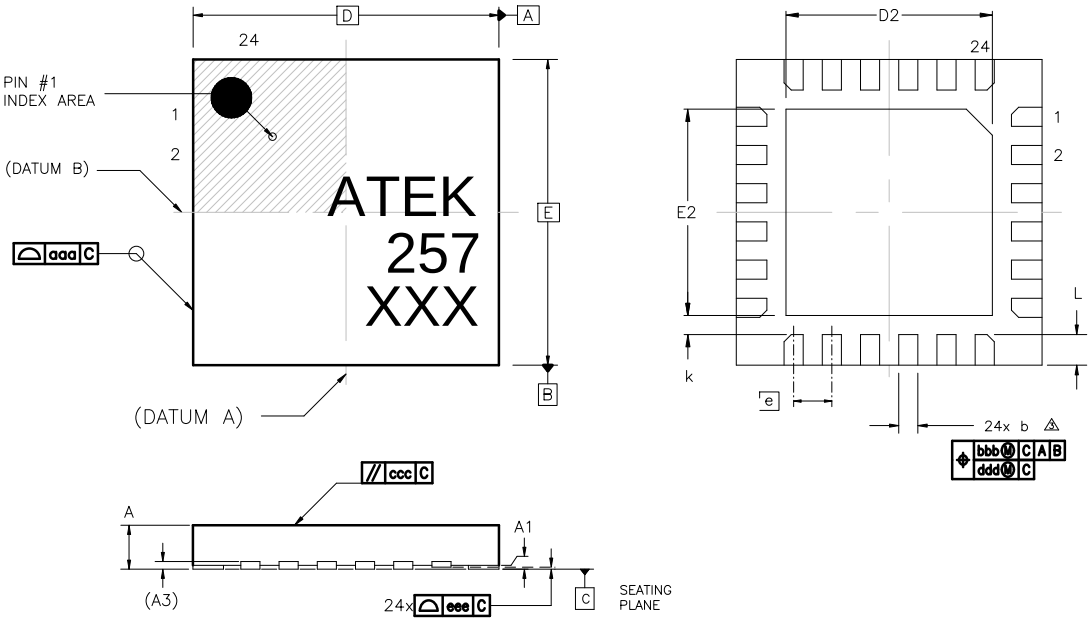
NC pins of the SP4T are connected to the GND on the EVB used to generate the plots shown in this document.

Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information



NOTES:
1) ALL DIMENSIONS IN MM
2) DIMENSIONING AND TOLERANCING PER ASME Y14.5–2009
3) DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
A, W	0.70	0.80	e	0.50 BSC	
A, L	1.40	1.70	k	0.20	–
A1	0.00	0.05	L	0.35	0.45
A3	0.20 REF		aaa	0.10	
b	0.18	0.30	bbb	0.10	
D	4.00 BSC		ccc	0.10	
D2	2.60	2.80	ddd	0.05	
E	4.00 BSC		eee	0.08	

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	02.08.2022	Initial Release	
1.1	07.09.2022	Format and Content Fixed	
1.2	28.03.2023	Pin Description Updated	