Product Description

ATEK256N3 is a wideband absorptive SPDT switch with low loss and high isolation. Frequency of operation starts from low frequencies close to DC, goes up to 20 GHz.

Operating with positive supply voltage and switch state is chosen by positive voltage control interface. Eliminates the need for external negative bias circuitry for the user.

RF input outputs are matched to 50 ohms internally. Switch is housed in a compact low cost 3x3 mm surface mount package.

Evaluation Board, bare die, custom package, and module options are available upon request.

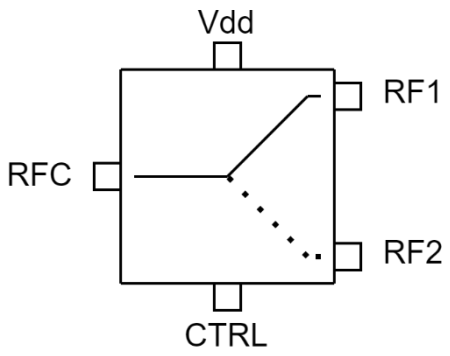
Product Features

- Frequency Range: LF - 20 GHz
- Insertion Loss: 1.8 dB at 10 GHz
- Input IP3: 40 dBm
- Positive Supply
- Positive Control
- 3x3 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test and Measurement
- SATCOM
- SDR

Functional Block Diagram



Electrical Specifications

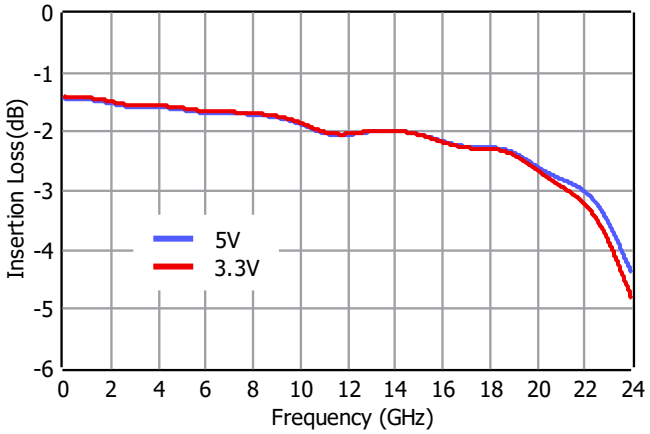
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		20	GHz
Insertion Loss	4 GHz		1.6		dB
	8 GHz		1.7		
	12 GHz		2.1		
	16 GHz		2.2		
	20 GHz		2.6		
Isolation	4 GHz		50		dB
	8 GHz		42		
	12 GHz		45		
	16 GHz		44		
	20 GHz		40		
Input Return Loss			-17		dB
Output Return Loss			-18		dB
Input IP3			40		dBm
Input P1dB			24		dBm
Switching Time	On		90		ns
	Off		25		
DC Supply Voltage (Vdd)			5		V
DC Supply Current			1		mA
Control Voltage (CTRL)	Low		0		V
	High		5		
Operating Temperature		-40		85	°C

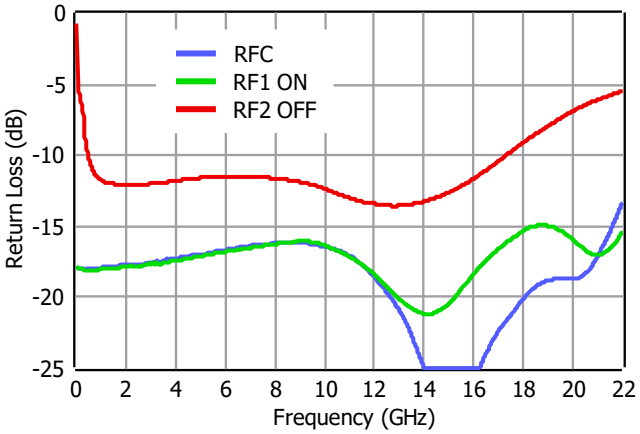
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

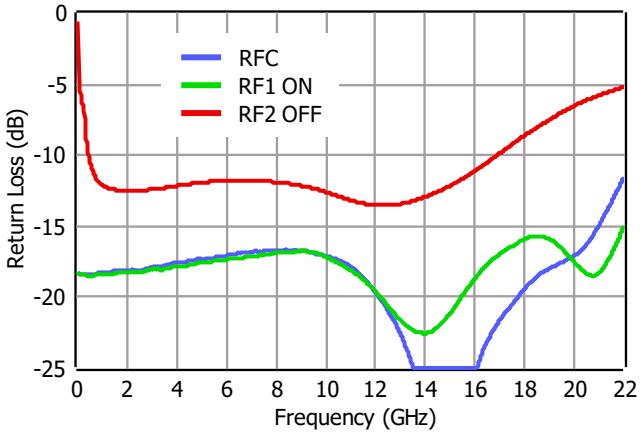
Insertion Loss



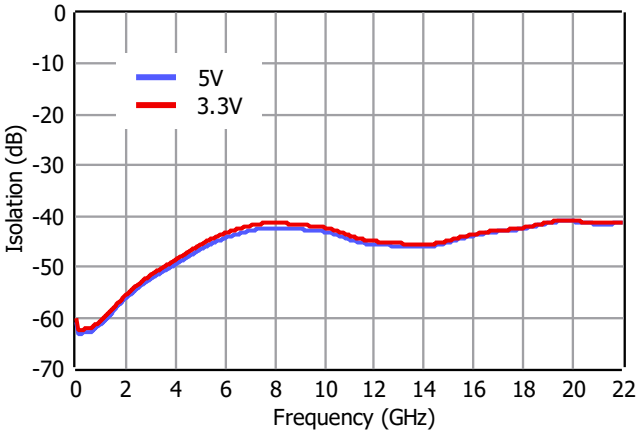
Return Loss at 5V



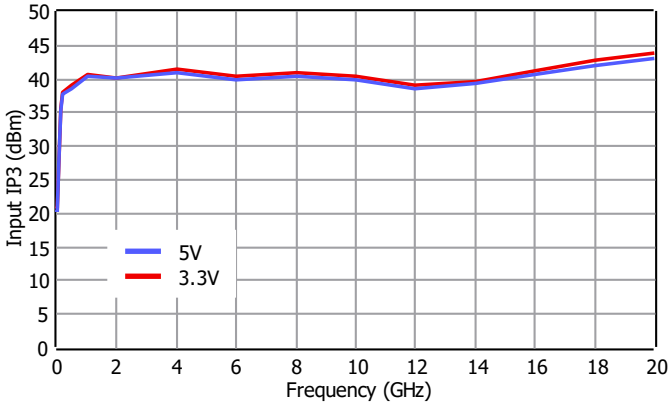
Return Loss at 3.3V



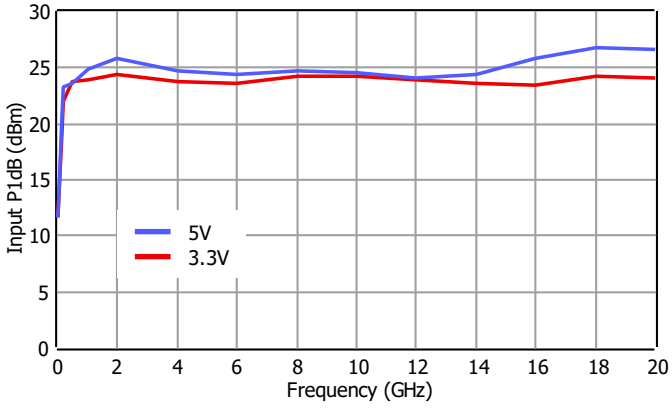
Isolation



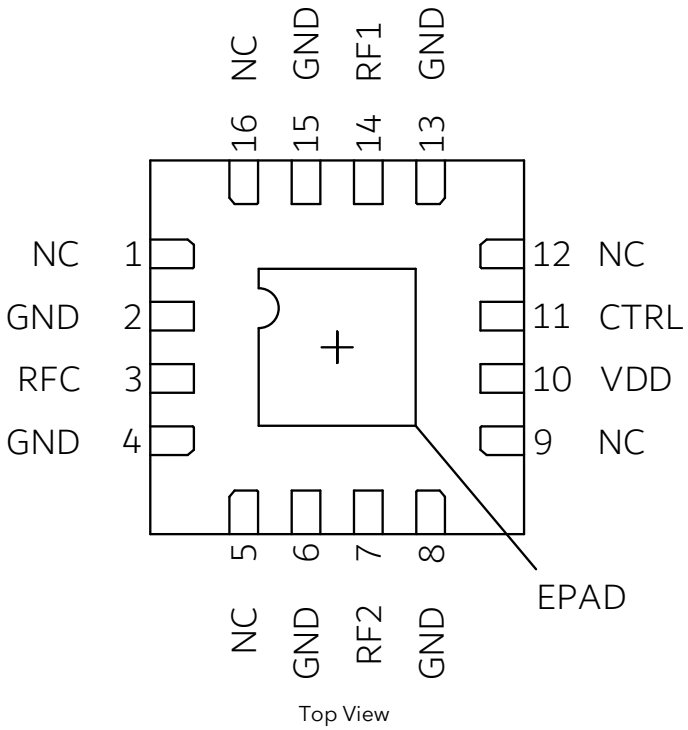
IIP3



P1dB



Pin Description



Top View

Pin Number	Pin Name	Description
3	RFC	RF input/output pin. Wideband DC block capacitor is required.
14	RF1	RF input/output pin. Wideband DC block capacitor is required.
7	RF2	RF input/output pin. Wideband DC block capacitor is required.
10	VDD	Supply input. Vdd bias pin.
11	CTRL	Control pin.
1, 5, 9, 12, 16	NC	These pins are not internally connected. Can be grounded on the PCB.
2, 4, 6, 8, 13, 15	GND	Ground.
17	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

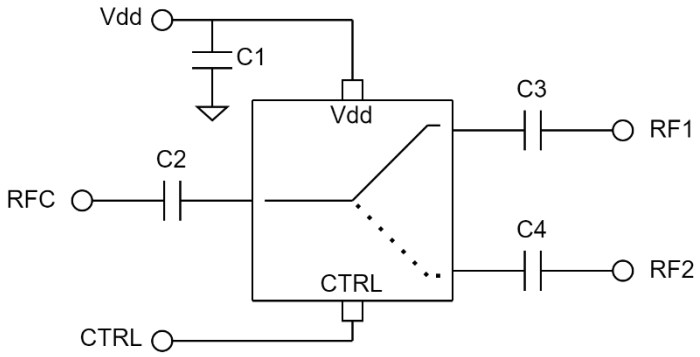
CTRLA	RFC to RF1	RFC to RF2
LOW	ON	OFF
HIGH	OFF	ON

Applications Information

Signal entering from RFC goes to RF1 or RF2 depending on the switch state set by the user.

Vdd bias is 5 V and control voltages are CMOS compatible. Switch state can be set by switching control voltages between 0 V to 5 V. Operating the switch is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the SPDT switch given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then SPDT can be operated without C1.

If needed, to filter out the ripples and unwanted signals on the external CTRL signal, a low pass filter in series R, shunt C configuration can be implemented on the CTRL line. Note that external RC filtering limits the state switching speed of the SPDT.

C2, C3 and C4 are wideband DC block capacitors.

CTRL voltage is used for setting the switch sate.

Large signal datasheet plots are generated by connectorized evaluation boards (EVBs), PCB and connector losses are de-embedded. Small signal plots are generated by probing the RF lines with RF probes to eliminate the connector transition effects.

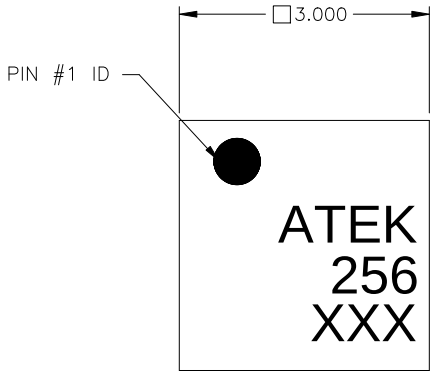
NC pins of the SPDT are connected to the GND on the EVBs used to generate the plots shown in this document.

Absolute Maximum Ratings

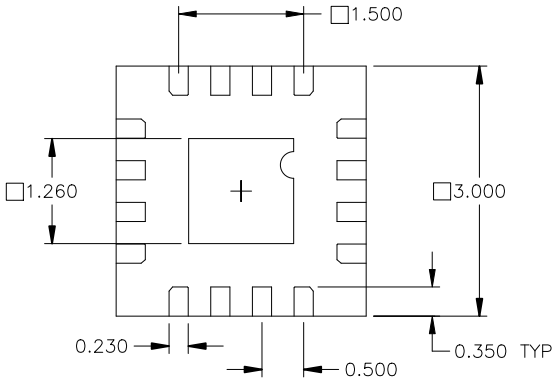
Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

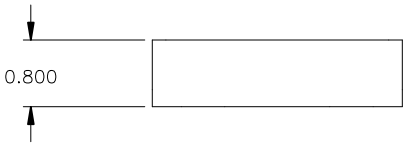
Mechanical and Marking Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES

1. JEDEC OUTLINE: MO−220
2. ALL DIMENSIONS IN MM
3. TOLERENCE IN X.XX= ±0.15 X.XXX= ±0.050

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Notice

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	30.05.2022	Initial Release	
1.1	24.05.2022	Control Interfaces Table Revised	
1.2	29.08.2024	Large Signal Data Added	