Product Description

ATEK255P4 is a wideband absorptive SP4T switch with low loss and high isolation. Frequency of operation starts from low frequencies close to DC, goes up to 12 GHz.

Operating from positive supply voltage and switch state is chosen by positive voltage control interface. Eliminates the need for external negative bias circuitry for the user.

RF input outputs are matched to 50 ohms internally. Switch is housed in a compact low cost 4x4 mm surface mount package.

Evaluation Board, bare die, custom package, and module options are available upon request.

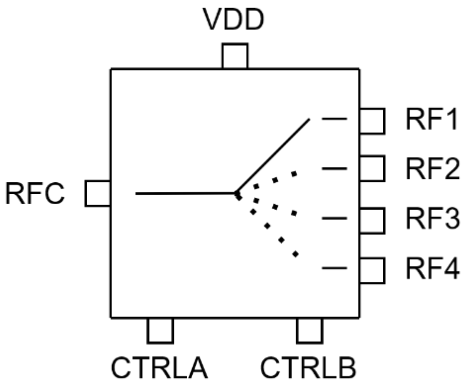
Product Features

- Frequency Range: LF – 12 GHz
- Insertion Loss: 2.2 dB at 6 GHz
- Positive Supply
- Positive Control
- IIP3: 45 dBm
- 4x4 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test Equipment
- Radar

Functional Block Diagram



Electrical Specifications

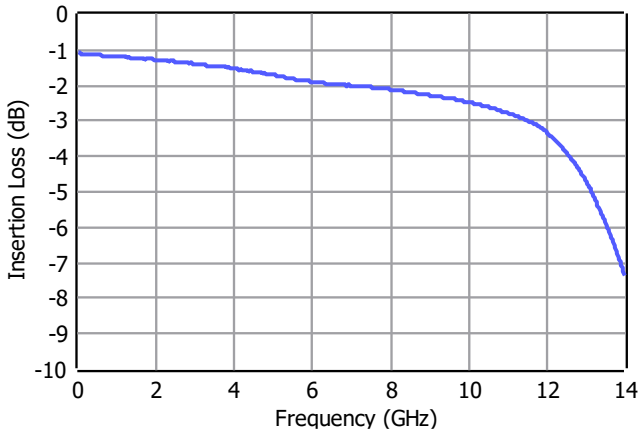
Conditions unless otherwise specified: V_{DD} = 5 V, T=25 C.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		12	GHz
Insertion Loss	2 GHz		1.4		dB
	4 GHz		1.8		
	6 GHz		2.2		
	10 GHz		3		
	12 GHz		4.2		
Isolation	2 GHz		54		dB
	4 GHz		44		
	6 GHz		38		
	10 GHz		33		
	12 GHz		30		
Input Return Loss			-14		dB
Output Return Loss			-18		dB
Input IP3			45		dBm
Input P1dB			28		dBm
DC Supply Voltage (Vdd)			5		V
DC Supply Current			3		mA
Control Voltage (CTRLA, CTRLB)	Low	0			V
	High			5	
Operating Temperature		-40		85	°C

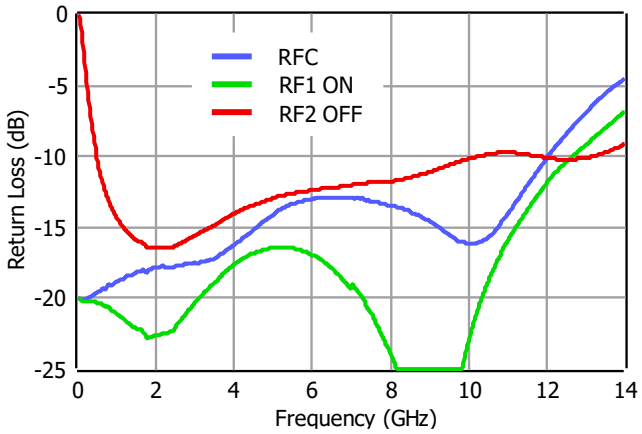
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T=25 C.

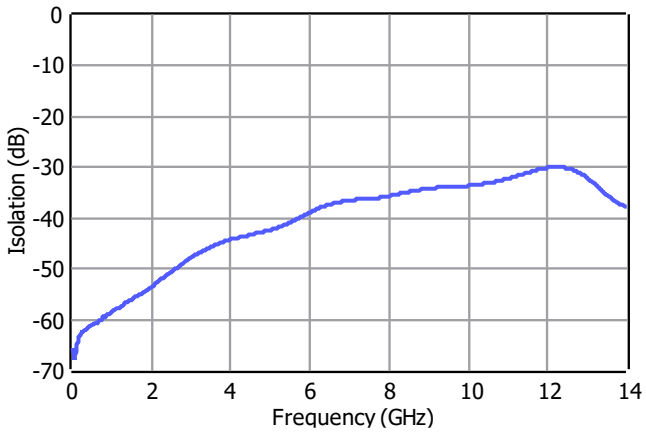
Insertion Loss



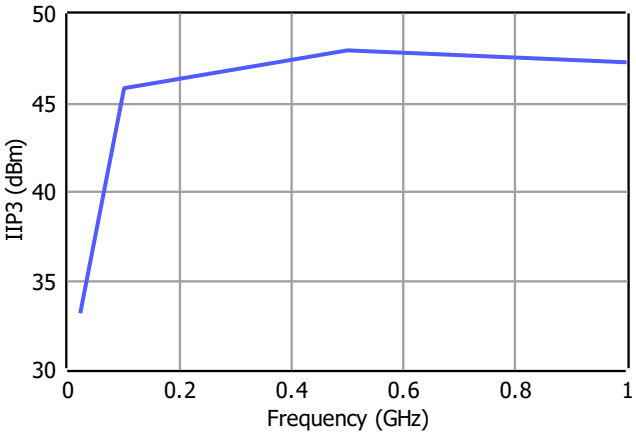
Return Loss



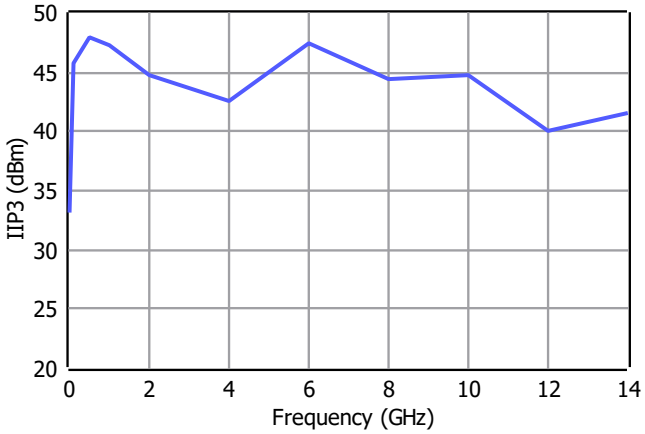
Isolation from RFC to RF2



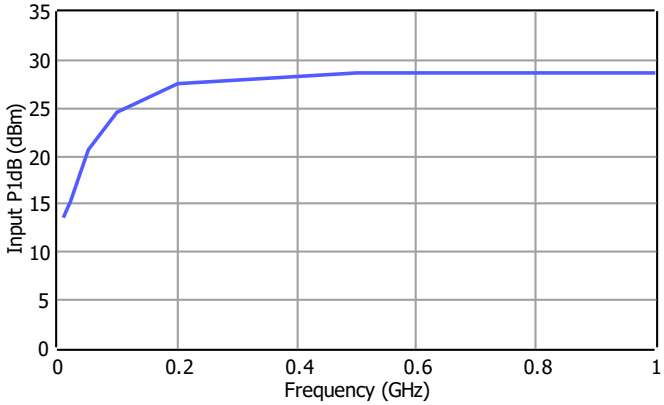
Input IP3 at Low Frequency



Input IP3 Wideband

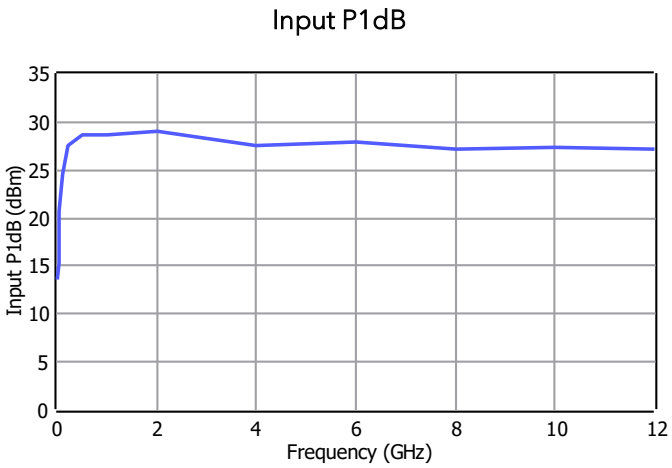


Input P1dB at Low Frequency

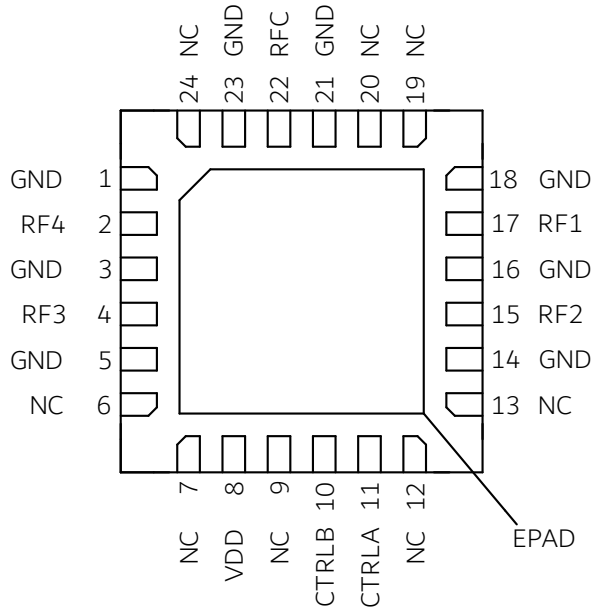


Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T=25 C.



Pin Description



Pin Number	Pin Name	Description
22	RFC	RF input/output pin. If the DC voltage level on RF line is not equal to 0 V, an external DC block capacitor is required.
17	RF1	RF input/output pin. If the DC voltage level on RF line is not equal to 0 V, an external DC block capacitor is required.
15	RF2	RF input/output pin. If the DC voltage level on RF line is not equal to 0 V, an external DC block capacitor is required.
4	RF3	RF input/output pin. If the DC voltage level on RF line is not equal to 0 V, an external DC block capacitor is required.
2	RF4	RF input/output pin. If the DC voltage level on RF line is not equal to 0 V, an external DC block capacitor is required.
11	CTRLA	Control pin.
10	CTRLB	Control pin.
8	VDD	Vdd bias pin.
6, 7, 9, 12, 13, 19, 20, 24	NC	These pins are not internally connected. Can be grounded on the PCB.
1, 3, 5, 14, 16, 18, 21, 23	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

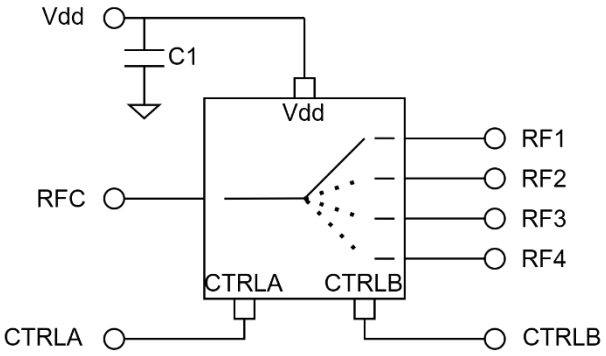
Control Interface

CTRLA	CTRLB	RFC to State
HIGH	HIGH	RF1
HIGH	LOW	RF2
LOW	HIGH	RF3
LOW	LOW	RF4

Applications Information

Signal entering from RFC goes to RF1-RF4 depending on the switch state set by the user.
Vdd bias is 5 V and control voltages are CMOS compatible. Switch state can be set by switching control voltages between 0 V to 5 V. Operating the switch is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the SP4T switch given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then SP4T can be operated without C1.

If needed, to filter out the ripples and unwanted signals on the external CTRL signals, a low pass filter in series R, shunt C configuration can be implemented on the CTRL lines. Note that external RC filtering limits the state switching speed of the SP4T.

CTRLA and CTRLB voltages are used for setting the switch state.

All datasheet plots are generated by a connectorized evaluation PCB with the application schematic provided above. Insertion Loss, Isolation and IP3 performance is measured with connectorized evaluation PCB. Then the loss of the PCB is de-embedded to generate the data presented in this document.

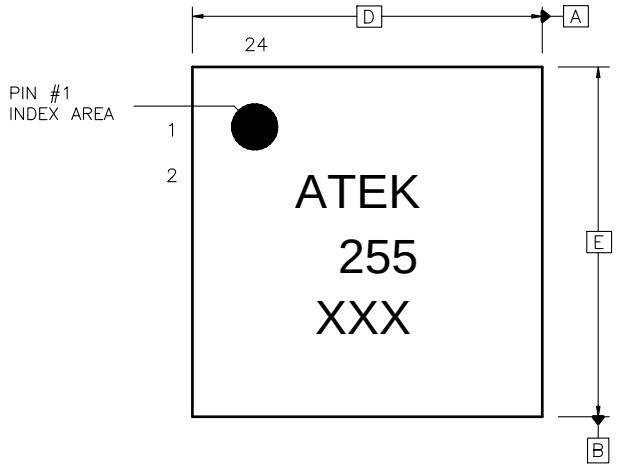
NC pins of the SP4T are connected to the GND on the EVB used to generate the plots shown in this document.

Absolute Maximum Ratings

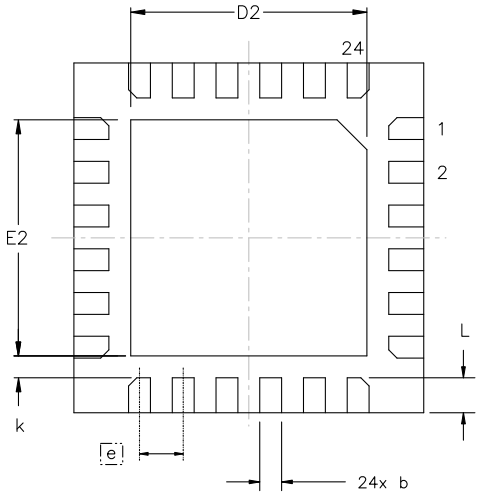
Parameter	Value/Range
Supply Voltage (Vdd)	TBD
Control Voltages (CTRLA, CTRLB)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

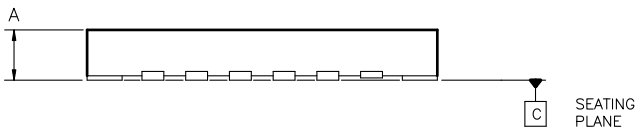
Mechanical and Marking Information



Top View



Bottom View



Side View

NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
b	0.18	0.30	e	0.50 BSC	
D	4.00 BSC		k	0.20	–
D2	2.60	2.80	L	0.35	0.45
E	4.00 BSC				

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	07.07.2021	Initial Version	
1.1	12.09.2023	Plots Added	