

Product Description

ATEK251P4 is a wideband absorptive SP8T switch with low loss and high isolation. Frequency of operation starts from low frequencies close to DC, goes up to 12 GHz.

Operating from positive supply voltage and switch state is chosen by positive voltage control interface. Eliminates the need for external negative bias circuitry for the user.

RF input outputs are matched to 50 ohms internally. Switch is housed in a compact low cost 4x4 mm surface mount package.

Evaluation Board, bare die, custom package, and module options are available upon request.

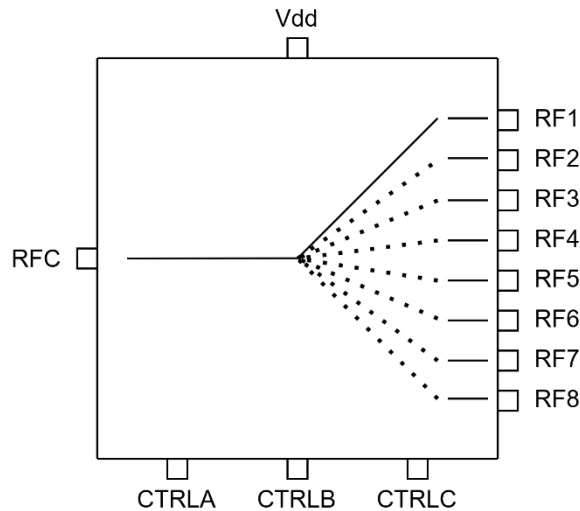
Product Features

- Frequency Range: LF - 12 GHz
- Insertion Loss: 2 dB
- Positive Supply
- Positive Control
- IIP3: 45 dBm
- 4x4 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test and Measurement
- Radar
- Electronic Warfare

Functional Block Diagram



Electrical Specifications

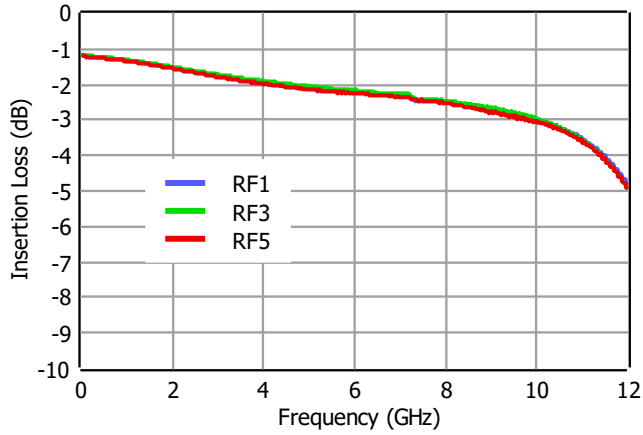
Conditions unless otherwise specified: $V_{DD} = 5V$, $T = 25\text{ C}$.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		12	GHz
Insertion Loss	2 GHz		1.5		dB
	4 GHz		1.9		
	6 GHz		2.2		
	10 GHz		3		
	12 GHz		4.9		
Isolation	2 GHz		65		dB
	4 GHz		55		
	6 GHz		48		
	10 GHz		33		
	12 GHz		26		
Input Return Loss			-14		dB
Output Return Loss			-14		dB
Input IP3			45		
DC Supply Voltage (Vdd)			5		V
DC Supply Current			4		mA
Control Voltage (CTRLA, CTRLB, CTRLC)	Low	0		1	V
	High	2		5	
Operating Temperature		-40		85	°C

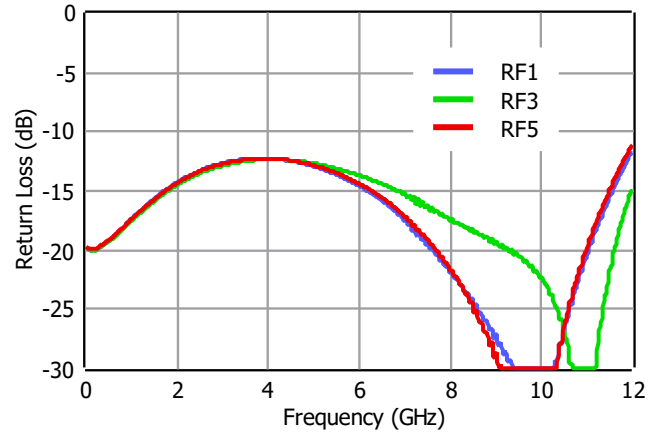
Typical Performance Plots

Conditions unless otherwise specified: $V_{DD} = 5\text{ V}$, $T=25\text{ C}$.

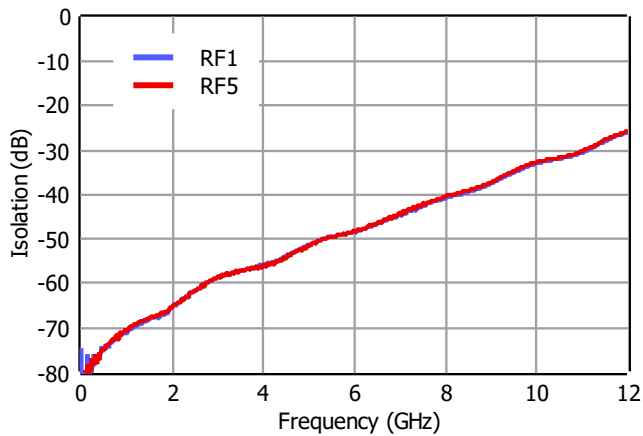
Insertion Loss



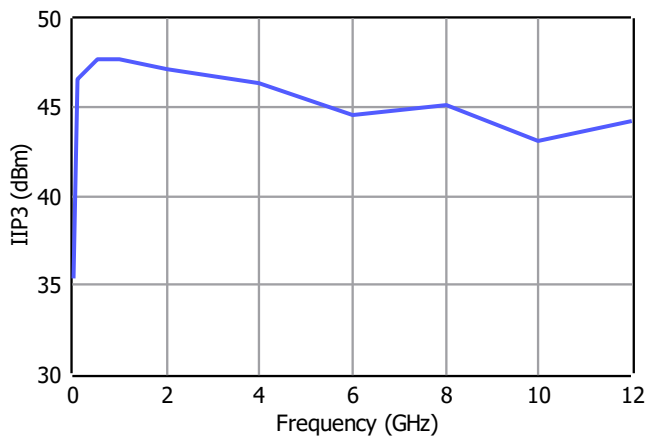
Return Loss



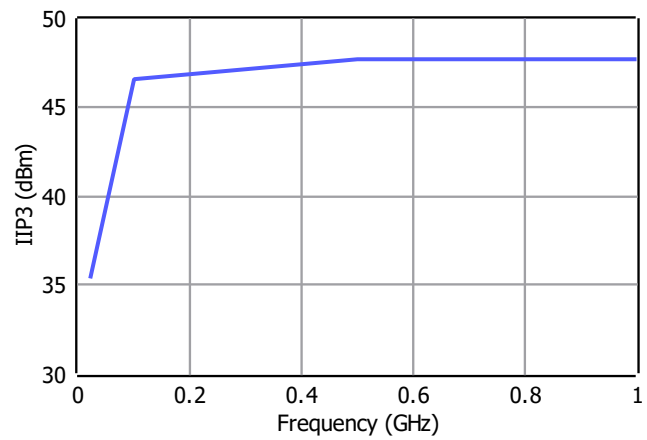
Isolation



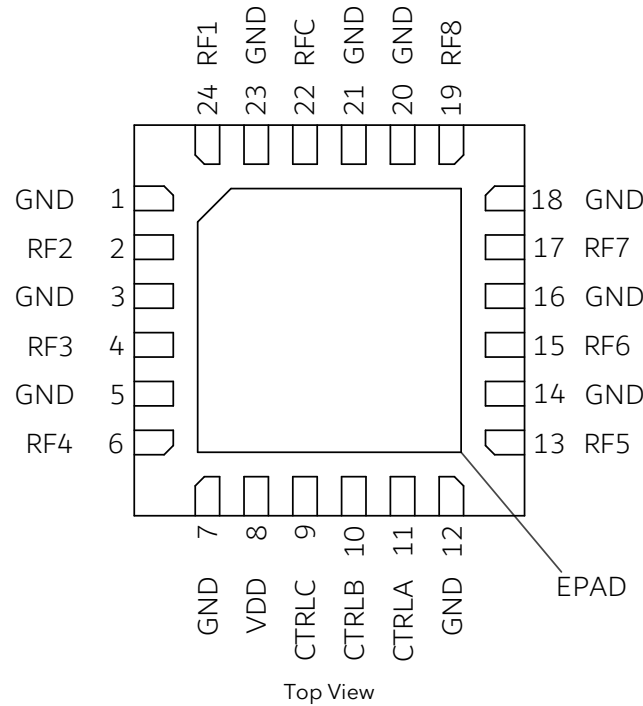
Input IP3 Wideband



Input IP3 Low Frequency



Pin Description



Pin Number	Pin Name	Description
22	RFC	RF input/output pin. Wideband DC block capacitor is required.
24	RF1	RF input/output pin. Wideband DC block capacitor is required.
2	RF2	RF input/output pin. Wideband DC block capacitor is required.
4	RF3	RF input/output pin. Wideband DC block capacitor is required.
6	RF4	RF input/output pin. Wideband DC block capacitor is required.
13	RF5	RF input/output pin. Wideband DC block capacitor is required.
15	RF6	RF input/output pin. Wideband DC block capacitor is required.
17	RF7	RF input/output pin. Wideband DC block capacitor is required.
19	RF8	RF input/output pin. Wideband DC block capacitor is required.
11	VDD	Vdd bias pin.
8	CTRLA	Control pin.
9	CTRLB	Control pin.
10	CTRLC	Control pin.
1, 3, 5, 7, 12, 14, 16, 18, 20, 21, 23	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

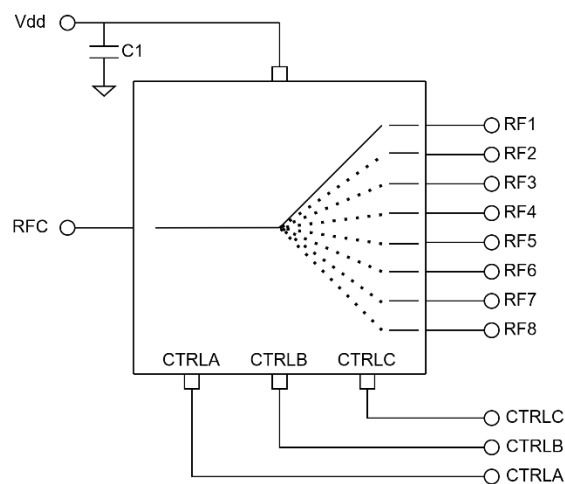
CTRLA	CTRLB	CTRLC	RFC to State
HIGH	HIGH	HIGH	RF1
HIGH	HIGH	LOW	RF2
HIGH	LOW	HIGH	RF3
HIGH	LOW	LOW	RF4
LOW	HIGH	HIGH	RF5
LOW	HIGH	LOW	RF6
LOW	LOW	HIGH	RF7
LOW	LOW	LOW	RF8

Applications Information

Signal entering from RFC goes to RF1-8 depending on the switch state set by the user.

Vdd bias is 5 V and control voltages are CMOS compatible. Switch state can be set by switching control voltages between 0 V to 5 V. Operating the switch is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the SP8T switch given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then SP8T can be operated without C1.

If needed, to filter out the ripples and unwanted signals on the external CTRL signals, a low pass filter in series R, shunt C configuration can be implemented on the CTRL lines. Note that external RC filtering limits the state switching speed of the SP4T.

CTRLA, CTRLB and CTRLC voltages are used for setting the switch state.

All datasheet plots are generated by a connectorized evaluation PCB with the application schematic provided above. Insertion Loss, Isolation and IP3 performance is measured with connectorized evaluation PCB. Then the loss of the PCB is de-embedded to generate the data presented in this document.

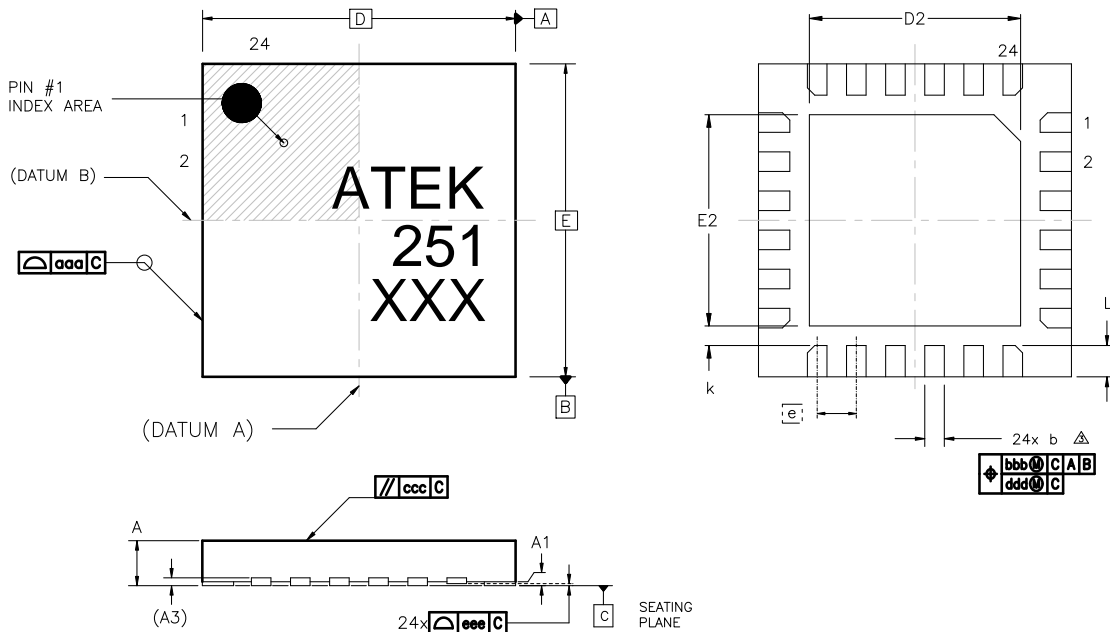
NC pins of the SP8T are connected to the GND on the EVB used to generate the plots shown in this document.

Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltage (Vdd)	TBD
Control Voltages (CTRLA, CTRLB, CTRLC)	TBD
RF Input Power	TBD
Storage Temperature	-55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

Mechanical and Marking Information



NOTES:
1) ALL DIMENSIONS IN MM
2) DIMENSIONING AND TOLERANCING PER ASME Y14.5-2009
3) DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
A, W	0.70	0.80	e	0.50	BSC
A, L	1.40	1.70	k	0.20	-
A1	0.00	0.05	L	0.35	0.45
A3	0.20	REF	aaa	0.10	
b	0.18	0.30	bbb	0.10	
D	4.00	BSC	ccc	0.10	
D2	2.60	2.80	ddd	0.05	
E	4.00	BSC	eee	0.08	

Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	29.01.2021	Initial Release	
1.1	11.07.2021	Drawing Updated	7/8
1.2	06.07.2022	Pin Description Updated	