Product Description

ATEK151P3 is a wideband low noise amplifier covering 0.01 to 3 GHz frequency range. Amplifier operational low frequency range can be extended to lower frequencies by increasing external component values.

ATEK151P3 provides flat gain and sub-1dB noise figure over wide bandwidth without the need for external matching components. This allows users to easily realize wideband receiver frontends.

Amplifier housed in compact 3x3 mm low cost SMD package, input and output matched to 50 ohms internally.

Evaluation Board, bare die, custom package, and module options are available upon request.

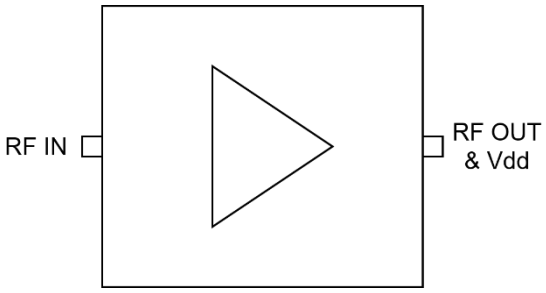
Product Features

- Frequency Range: 10MHz - 3 GHz
- Gain: 20 dB
- Noise Figure: 0.8 dB
- P1dB: 20 dBm
- Single Supply
- 3x3 mm compact size

Applications

- Spectrum Analysis
- Wideband receivers
- Telecommunication
- Test Equipment
- SDR

Functional Block Diagram



Electrical Specifications

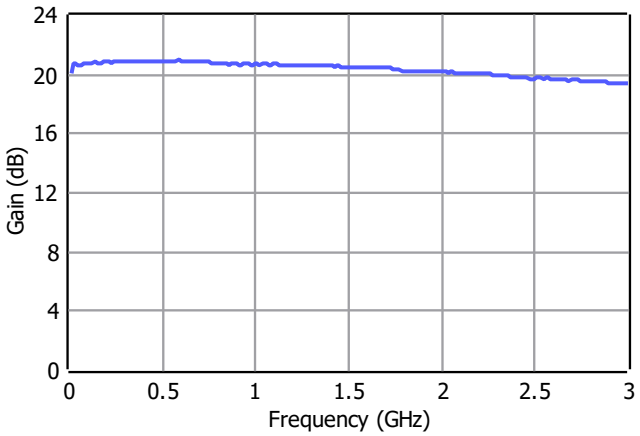
Conditions unless otherwise specified: V_{DD} = 5 V, T=25 C.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.01		3	GHz
Gain	10 MHz		20		dB
	0.5 GHz		20.8		
	1 GHz		20.7		
	2 GHz		20.1		
	3 GHz		19.3		
Noise Figure V_{DD} = 3.3 V	10 MHz		0.9		dB
	0.5 GHz		0.6		
	1 GHz		0.7		
	2 GHz		1		
	3 GHz		1.1		
Input Return Loss			9		dB
Output Return Loss			10		dB
Output P1dB			20		dBm
Output IP3			32		dBm
DC Supply Voltage			5		V
DC Supply Current			60		mA
Operating Temperature		-40		85	°C

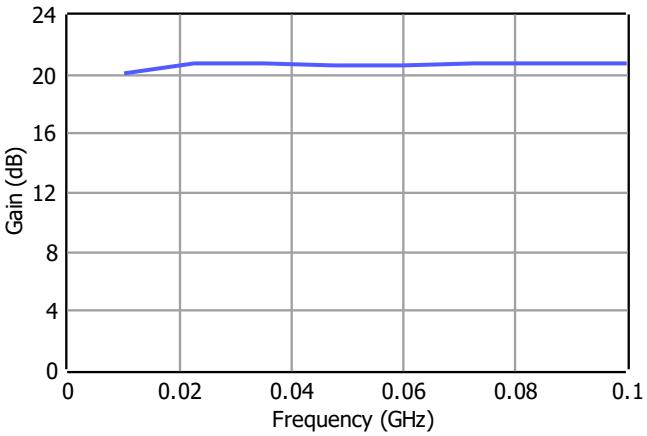
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T=25 C.

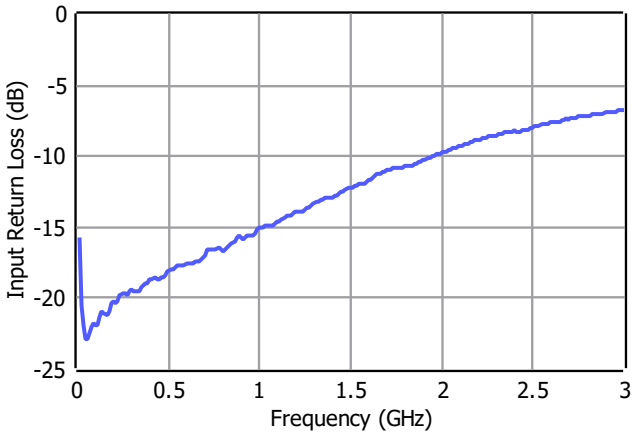
Gain



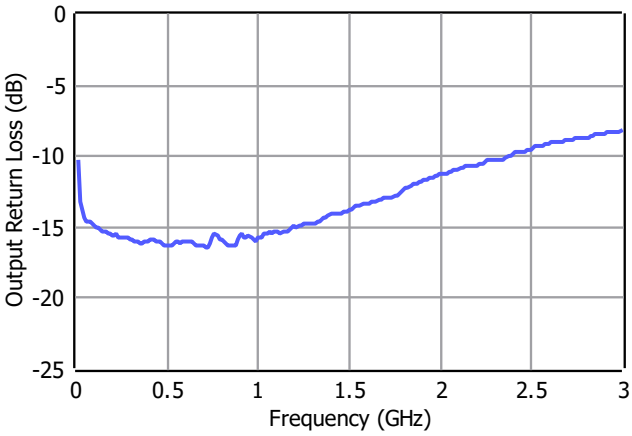
Gain – Low Frequency



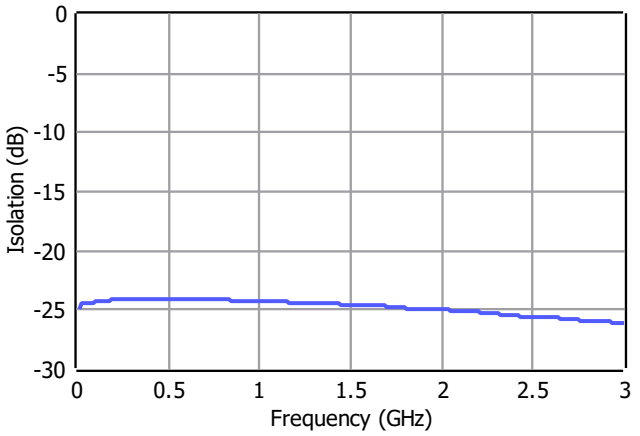
Input Return Loss



Output Return Loss



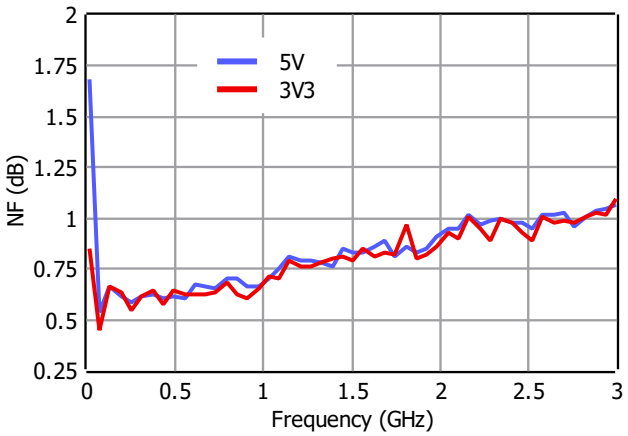
Isolation



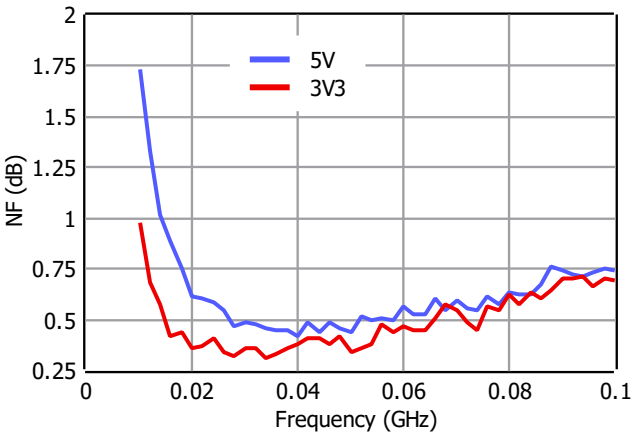
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T=25 C.

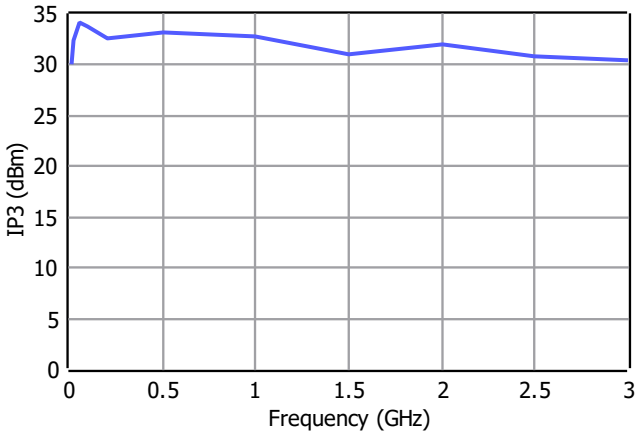
Noise Figure



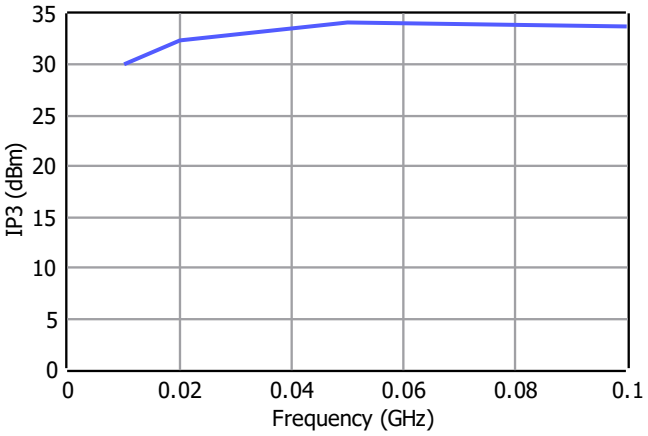
Noise Figure – Low Frequency



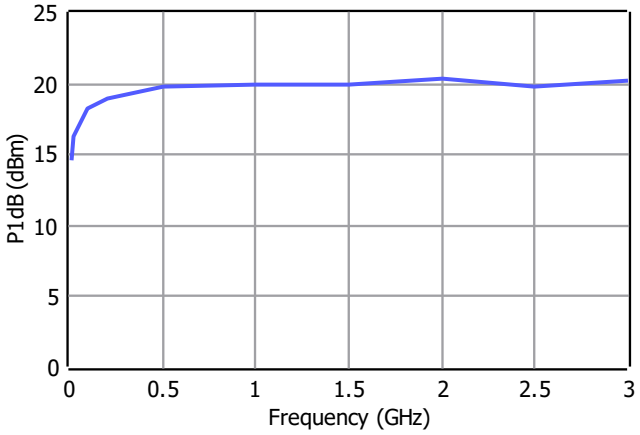
IP3



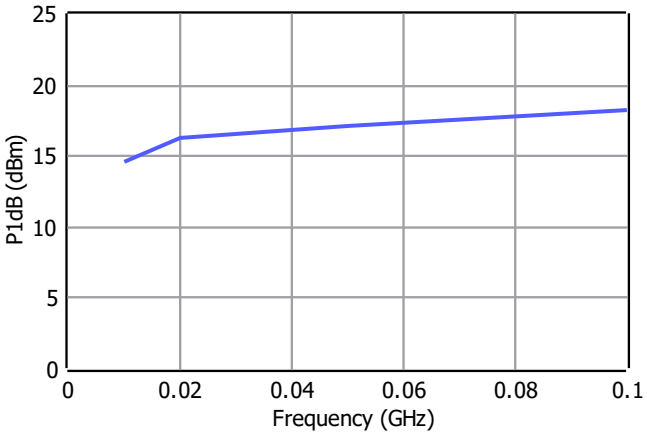
IP3 - Low Frequency



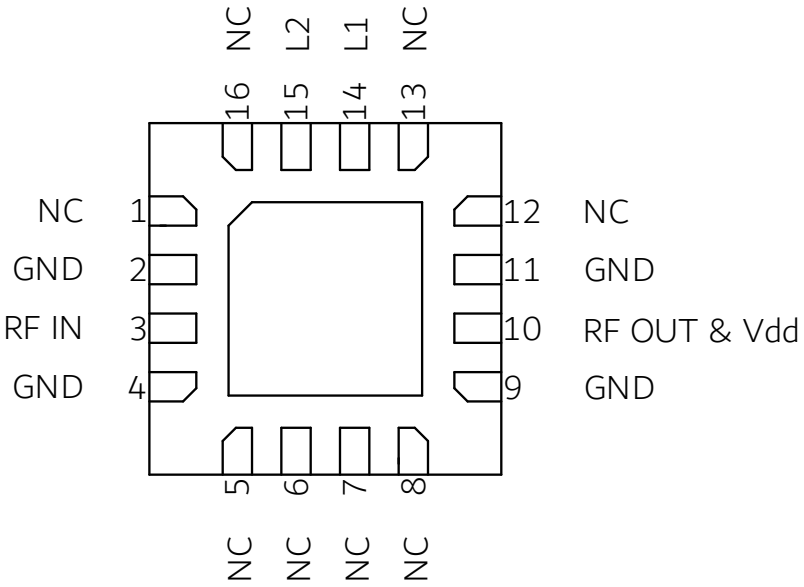
P1dB



P1dB – Low Frequency



Pin Description



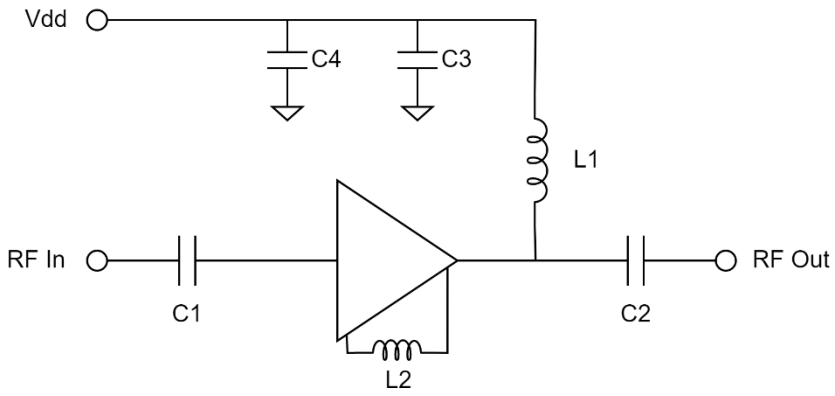
Top View

Pin Number	Pin Name	Description
3	RF IN	RF input pin. Wideband external DC block capacitor is required.
10	RF OUT & Vdd	RF output pin. Wideband external DC block capacitor is required.
14	L1	External inductor connection.
15	L2	External İnductor connection.
1, 5-8, 12, 13, 16	NC	These pins are not internally connected. Can be grounded on the PCB.
2, 4, 9, 11	GND	Ground.
17	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Applications Information

Signal entering from RF IN goes to RF OUT with an amplification.

Typical application schematic to operate the amplifier is given below.



C1 and C2 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss.

L1 is used as RF choke inductor. It is recommended to use wideband RF choke to achieve wideband performance.

Choosing higher values for C1, C2 and L1 will allow amplifier to operate at lower frequencies, compared to the plots that is given in this datasheet. By increasing values of these components, low frequency operation can be extended below 10 MHz, at the expense of flat wideband, and high frequency response.

C3 and C4 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C3 and C4 will improve this filtering. If this filtering is of no concern, then amplifier can be operated without C3 and C4.

L2 inductor is wideband RF choke type inductor.

Noise figure data is generated with connectorized evaluation PCB measurements. Then the input loss of the PCB is de-embedded from the noise figure measurement data across frequency, to generate the noise figure data shown in this document.

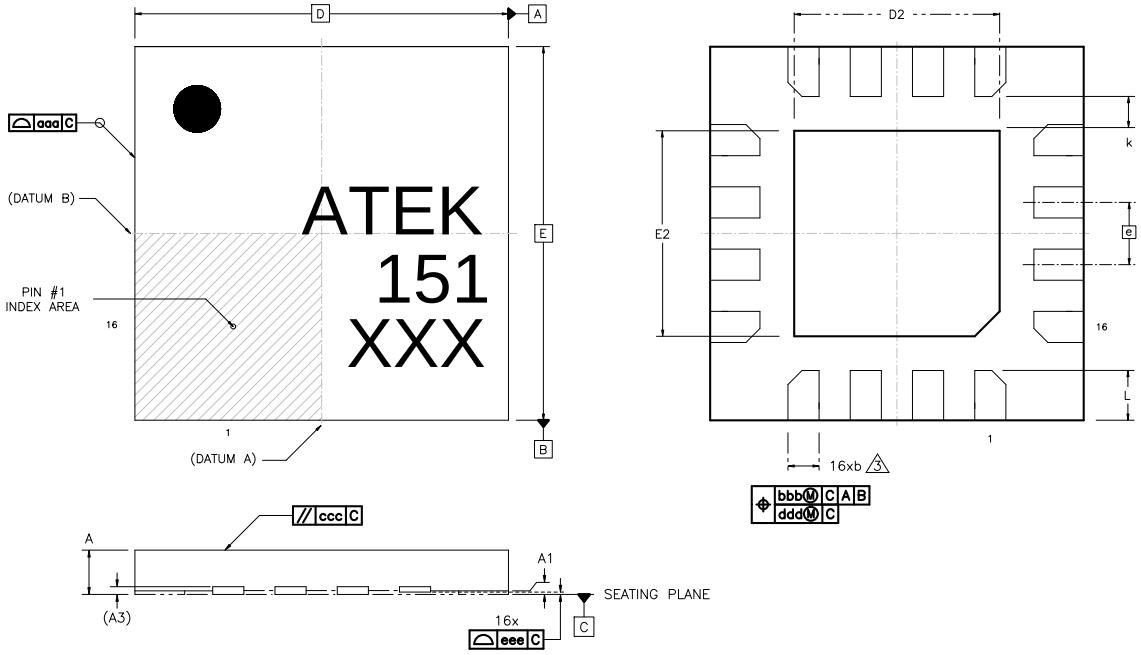
The NC pins of the Amplifier are connected to the GND on the PCBs used to generate the plots shown in this document. Vdd values shown on the datasheet correspond the Vdd pins shown on the application schematic, not the Vdd pin of the amplifier. Vdd value can be increased to get higher P1dB performance.

Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltages (Vdd1, Vdd2)	TBD
Gate Bias Voltages (Vgg1, Vgg2)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

Mechanical and Marking Information



NOTES:
1) ALL DIMENSIONS IN MM
2) DIMENSIONING AND TOLERANCING PER ASME Y14.5–2009
3) DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	1.55	1.75
A, W	0.70	0.80	e	0.50 BSC	
A, L	1.40	1.70	k	0.20	–
A1	0.00	0.05	L	0.35	0.45
A3	0.20 REF		aaa	0.10	
b	0.18	0.30	bbb	0.10	
D	3.00 BSC		ccc	0.10	
D2	1.55	1.75	ddd	0.05	
E	3.00 BSC		eee	0.08	

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	30.04.2022	Initial Release	
1.1	06.05.2022	Format and Content Fixed	
1.2	10.08.2022	Pin Description Revised	
1.3	06.09.2022	Format and Content Fixed	