User Guide
EVB-ATEK900N3-01

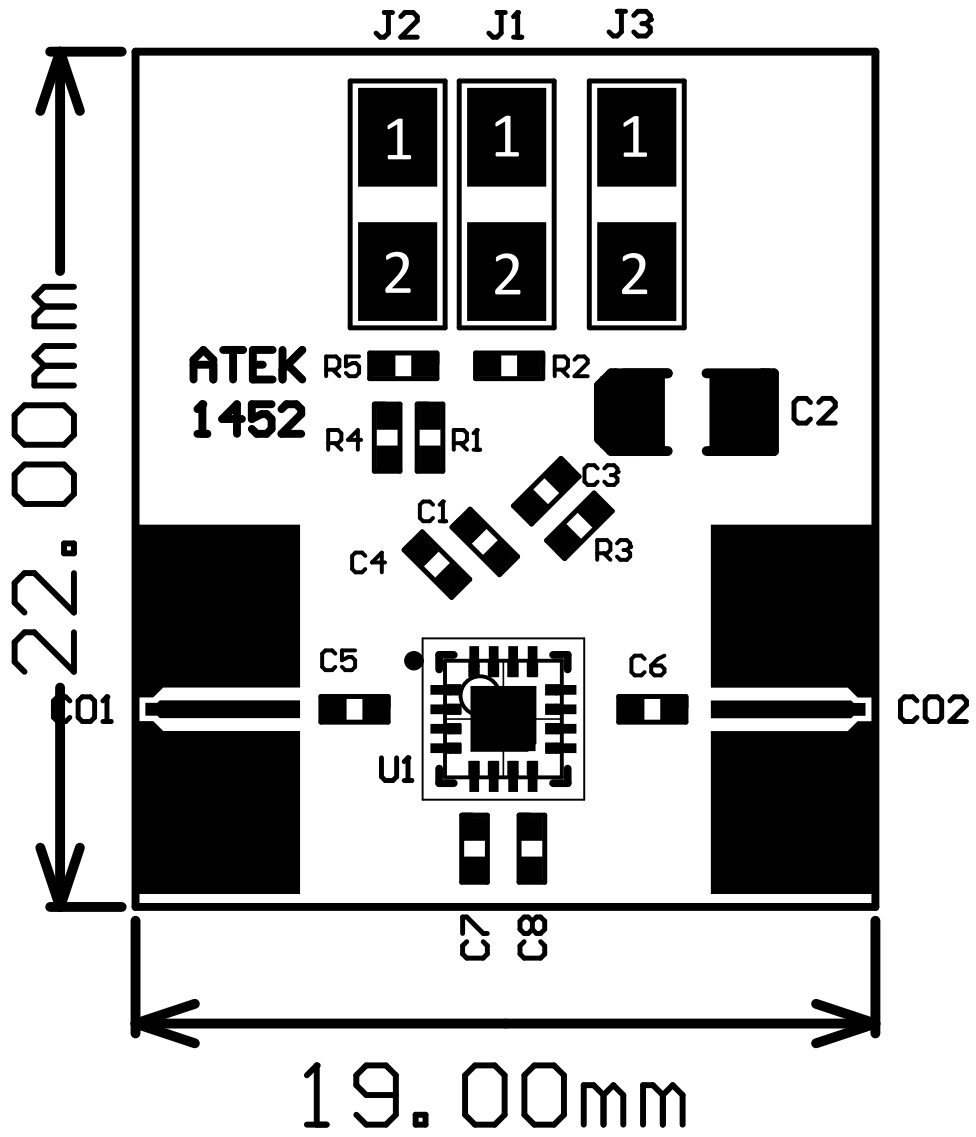
Document Code	: 023-145201
Revision No	: 04
Revision Date	: 28/07/2025

Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	13.03.2022	Initial Release	
1.1	16.04.2022	Format and Content Fixed	
1.2	26.07.2023	Pin Definition Revised	
1.3	28.07.2025	Pin Definition Revised	

INDEX

1 GENERAL INFORMATION



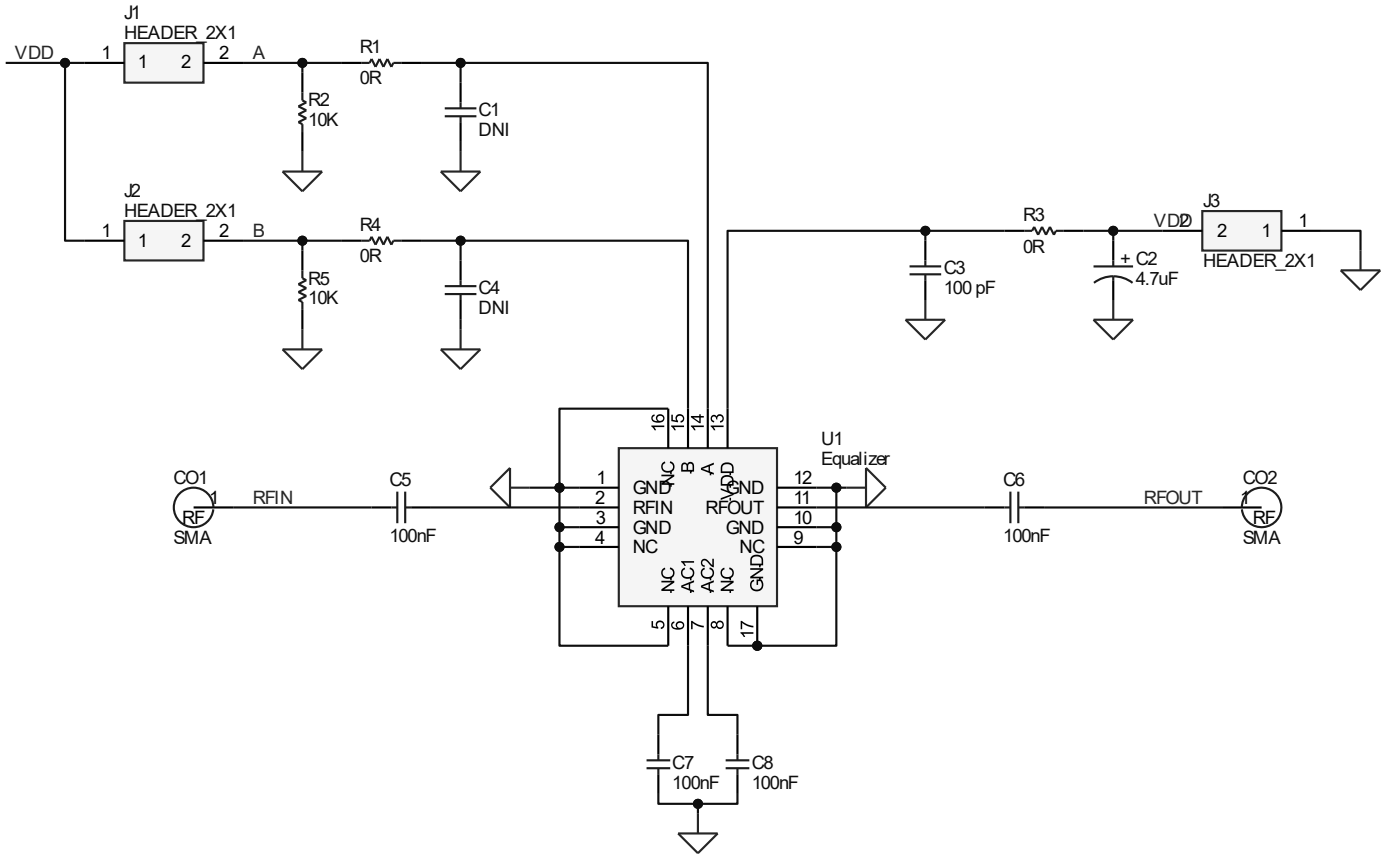
PIN Name	Definition	Comment
CO1	RF IN	K Connector
CO2	RF OUT	K Connector
J1.1, J2.1, J3.2	VDD	2.54mm Header
J1.2	CTRLA	2.54mm Header
J2.2	CTRLB	2.54mm Header
J3.1	GND	2.54mm Header

Notes:

1. Refer to the datasheet for VDD and Control Voltages details.

2 DESIGN INFORMATION

2.1 SCHEMATIC



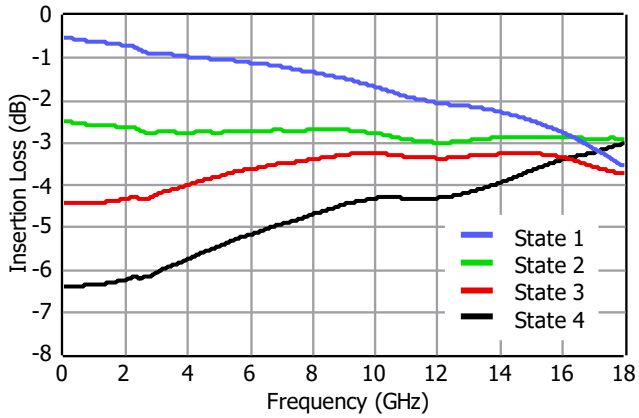
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C4	0402	2	DNP	
C2	CASEA	1	2.2uF	
C3	0402	1	100pF	
C5, C6	0402	2	100nF	
C7, C8	0402	2	100nF	
CO1, CO2	K Connector	2	K Connector	ATEK9292
J1, J2, J3	2x1 Header	3	2x1 Header	
R1, R3, R4	0402	3	0R	
R2, R5	0402	2	10k	
U1	ATEKQ3316	1	Equalizer	ATEK900N3

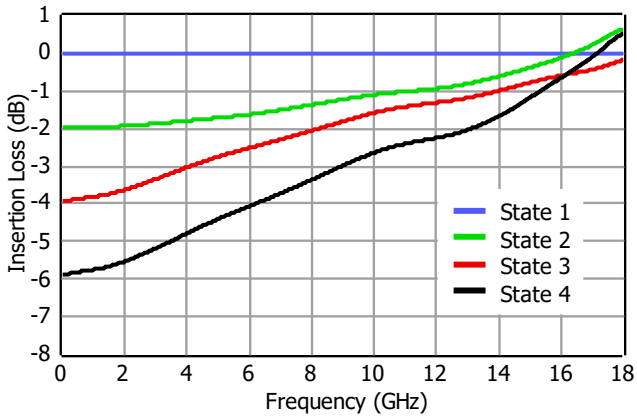
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: V_{CTRL} =0/5 V, T = 25 C, CW. For details, please refer to the datasheet.

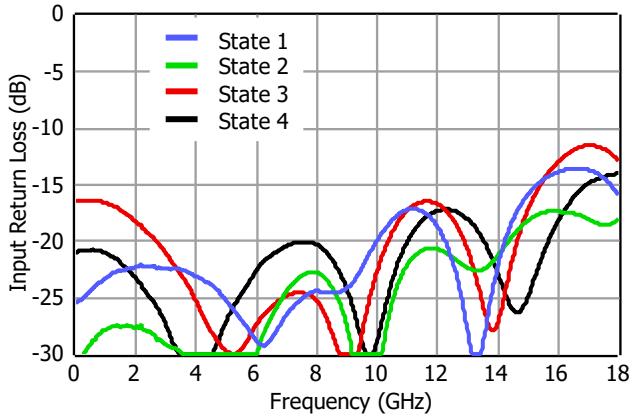
Insertion Loss



Normalized Equalization



Input Return Loss



Output Return Loss